

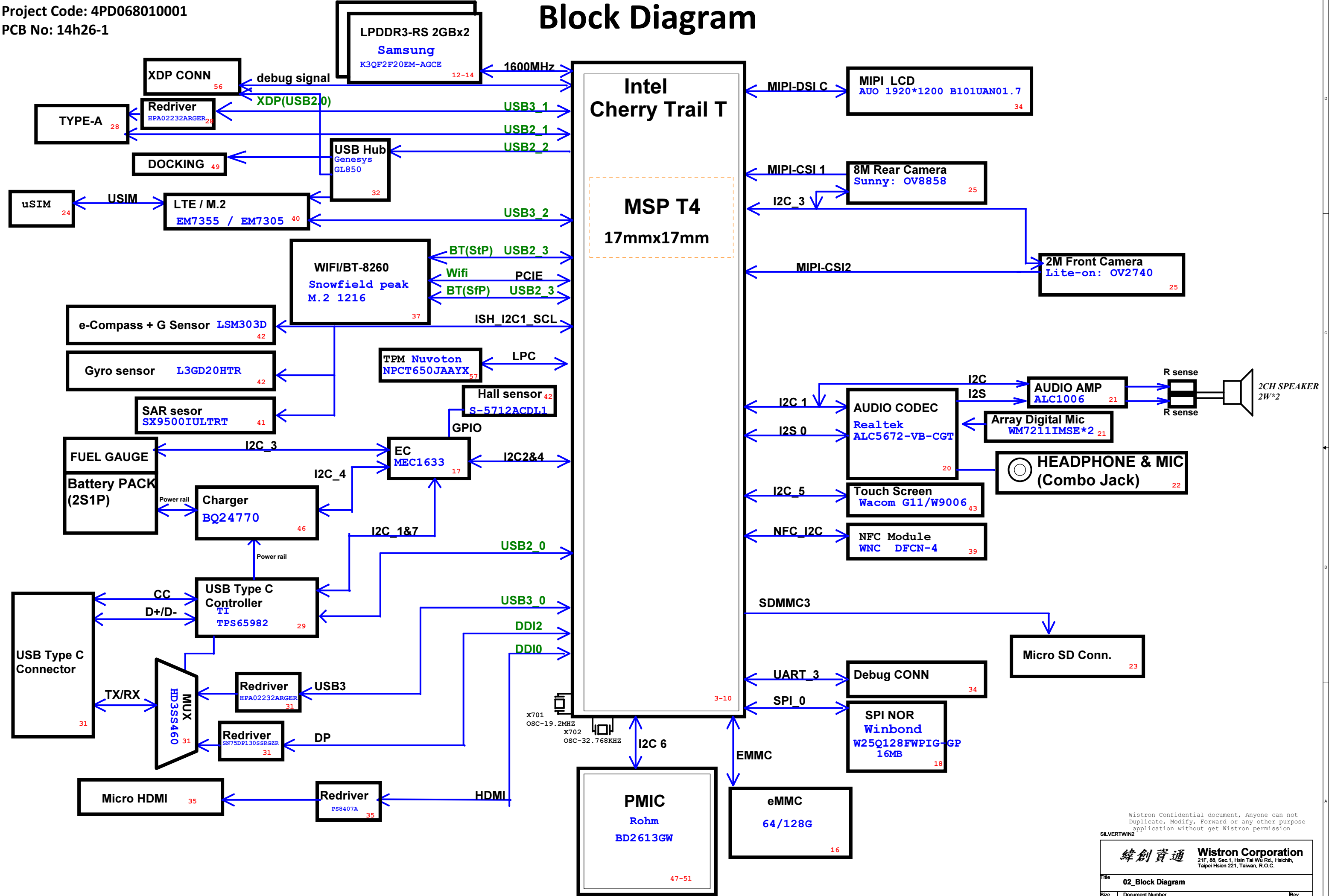
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Title01_Cover		
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Date: Sunday, September 27, 2015		Sheet 1 of 72

# Block Diagram



## 20130923 modify



#### 3.3.1.1.2 LPDDR3 Bit and Byte Lane Swapping

- If swapping is used, DQ signals within a channel must match its associate DQS/DQS# and DM signals.

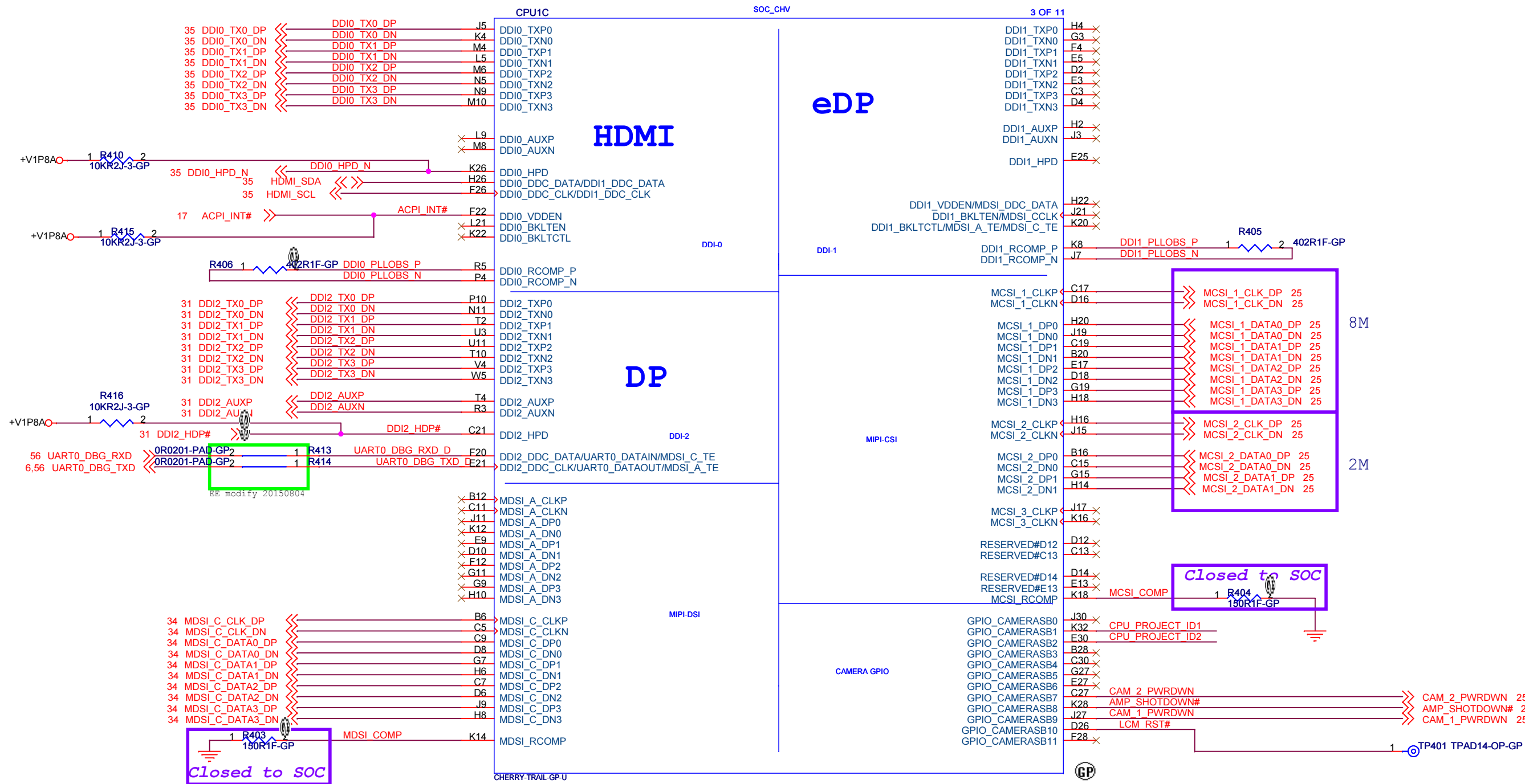
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Date:	Sunday, September 27, 2015	Sheet 3 of 72

e

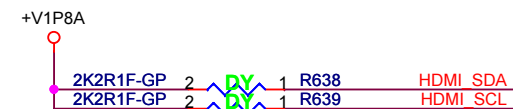
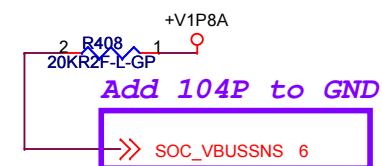
## SOC : DDI 0&1 / MIPI-DIS/MIPI-CSI/MIPI-GPIO



## PROJECT ID

EE modify 20150618

PROJECT	PROJECT_ID2	PROJECT_ID1
Blackwell-T3	0	0
Blackwell-T4	0	1
Somerset-T3	1	0
Somerset-T4	1	1



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SA

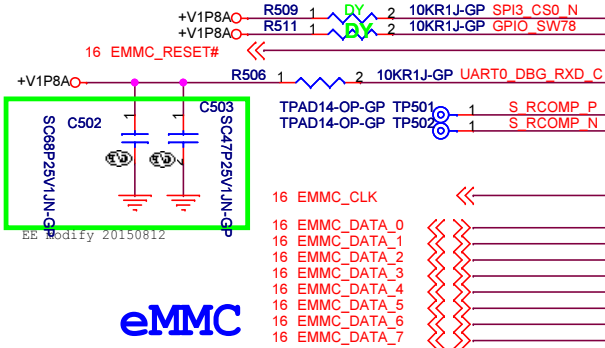
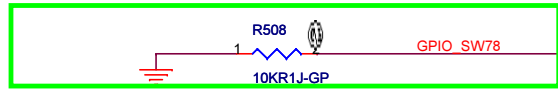
Date: Sunday, September 27, 2015

Sheet 4 of 72

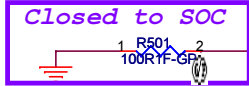


SOC : eMMC/SD/GPIO/I2S

EE modify 20150813  
BGM control!!  
WWAN : PD  
Non-WWAN: PH

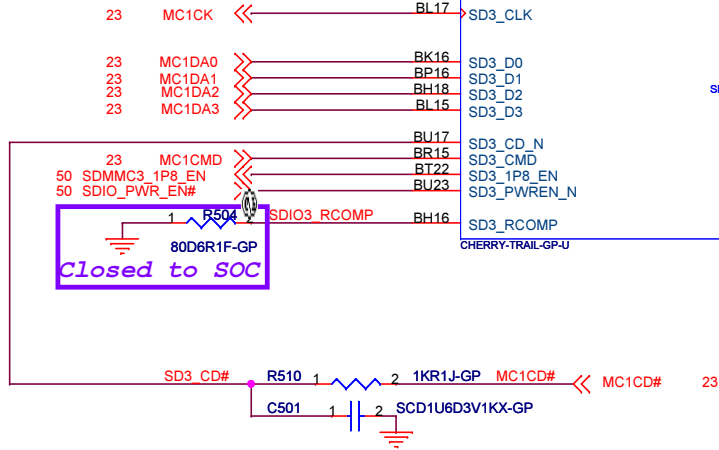


eMMC

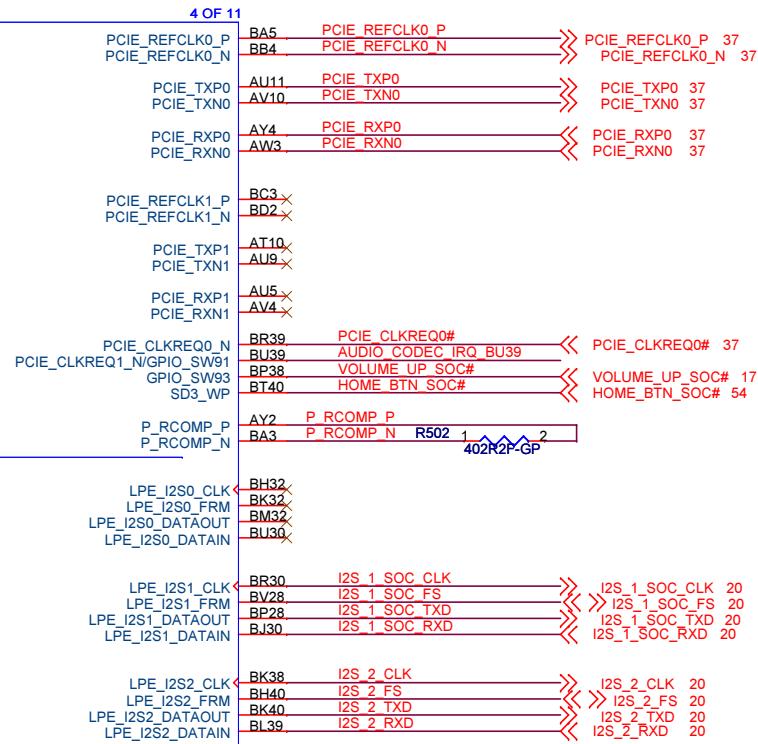
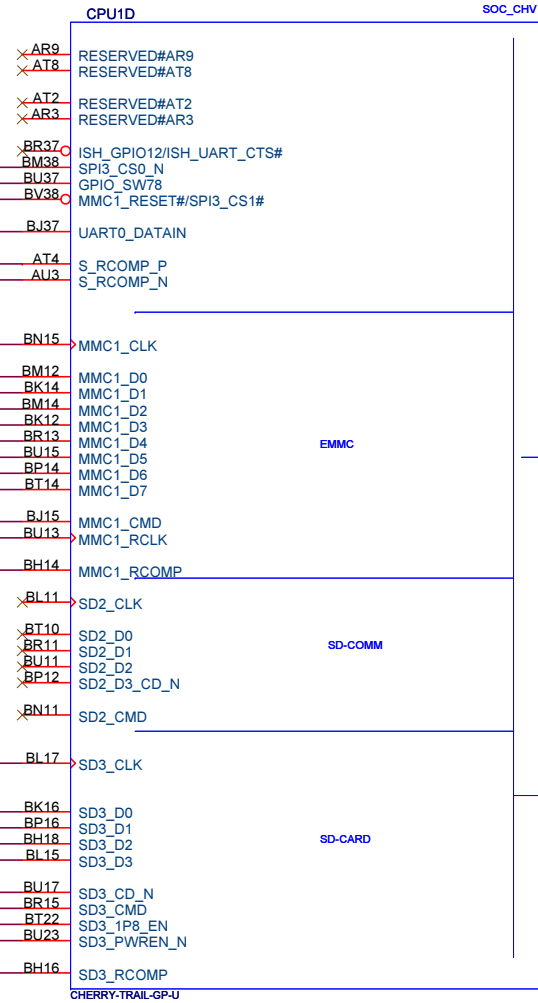
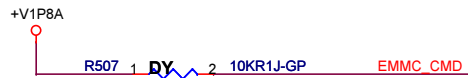


Closed to SOC

uSD



Closed to SOC

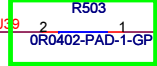


WI-FI

Audio Codec(DY)

Audio Codec

EE modify 20150804



AUDIO\_CODEC\_IRQ

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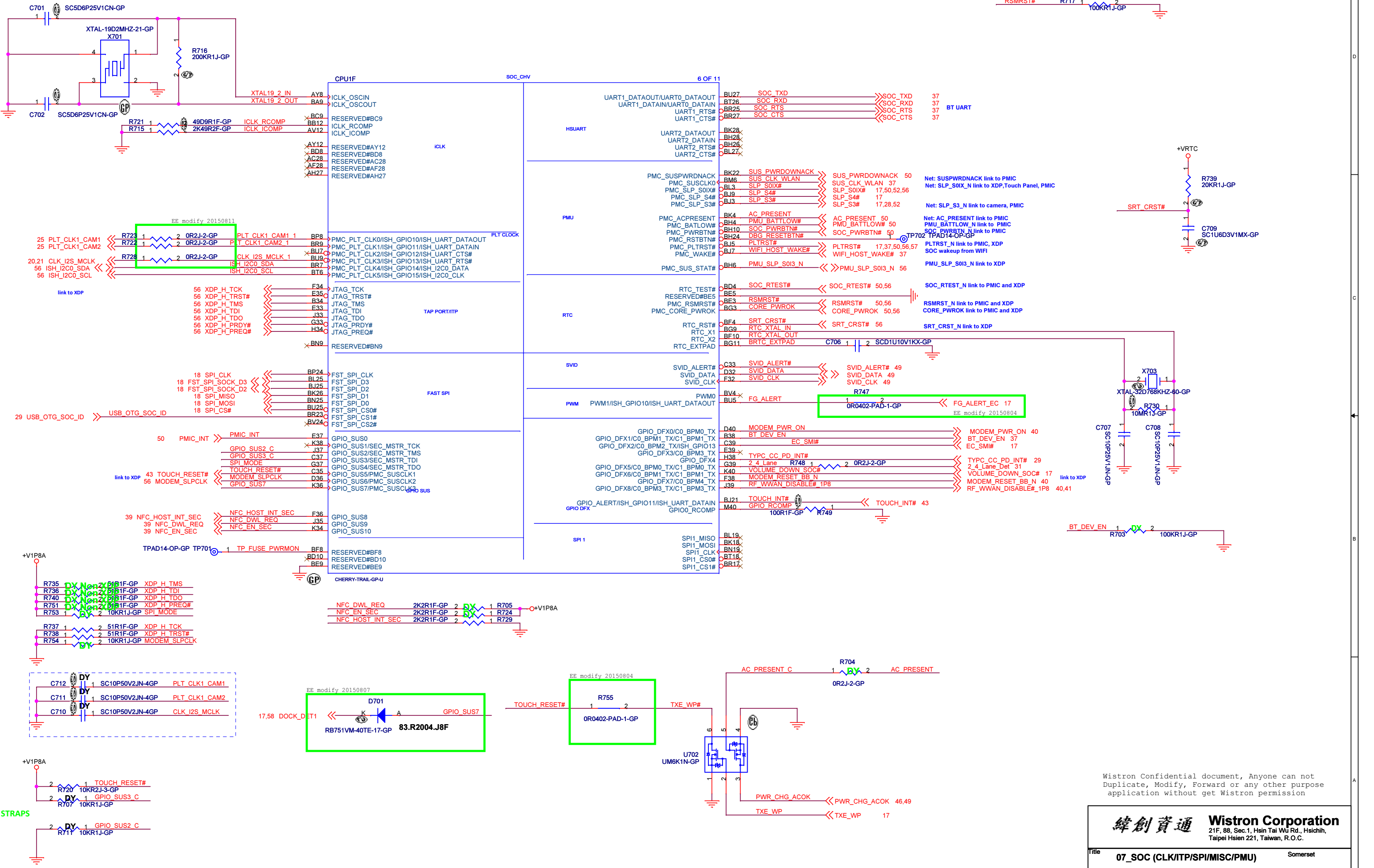
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Title 05_SOC (EMMC/SD/GPIO/I2S)		
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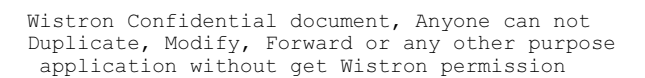
 <div> <b>Wistron Corporation</b>                  21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,                  Taipei Hsien 221, Taiwan, R.O.C.             </div>	
Title <b>06_SOC (USB/HSIC/LPC/HIS/I2C)</b>	
Size <b>Document Number</b> <b>Somerset</b>	Rev <b>SA</b>
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SOC : CLK/ITP/SPI NOR/GPIO SUS/HSUART/PMU/RTC



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## 20130924 modify



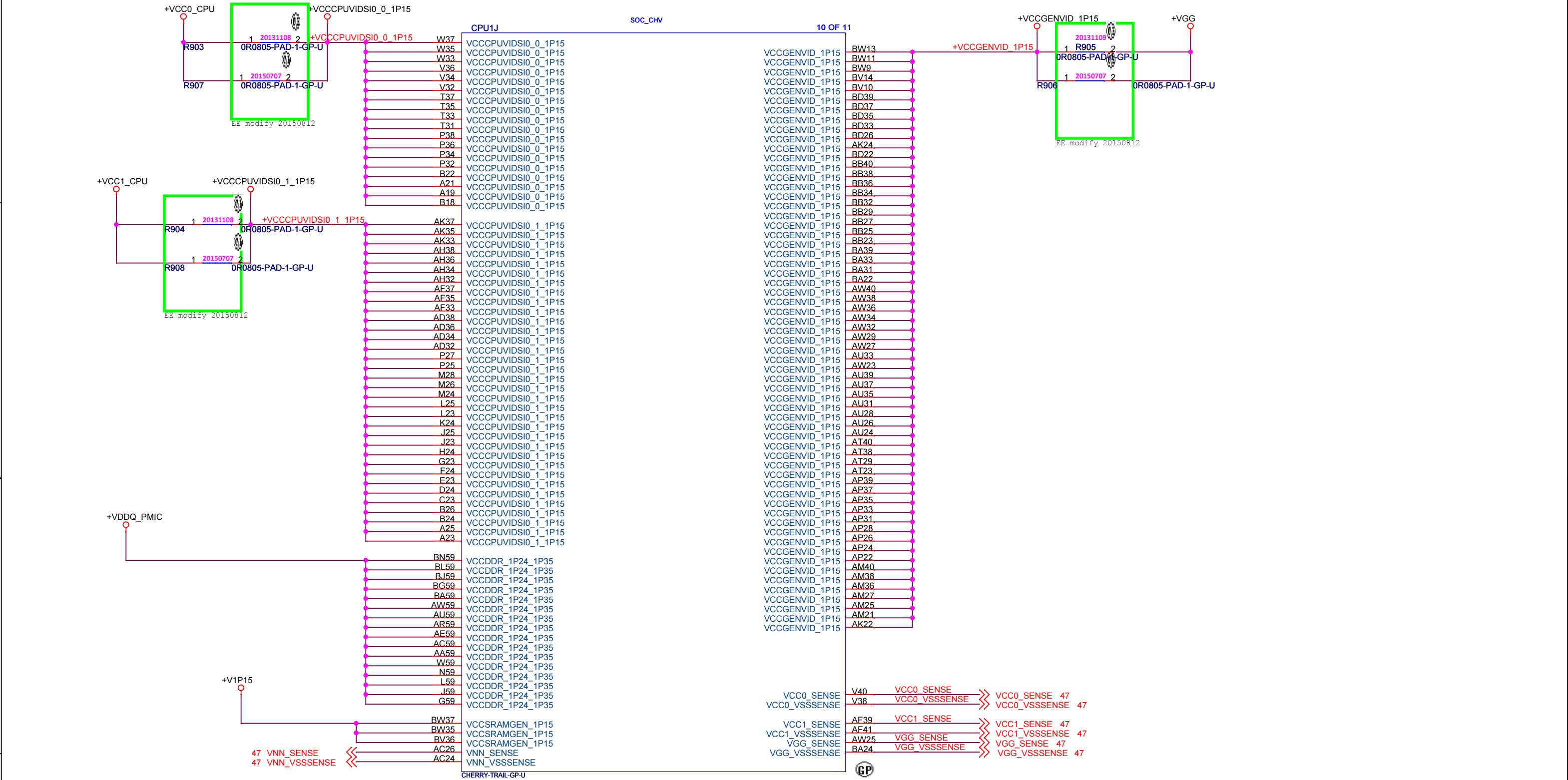
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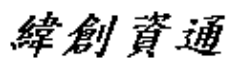


SOC : VCC/VNN



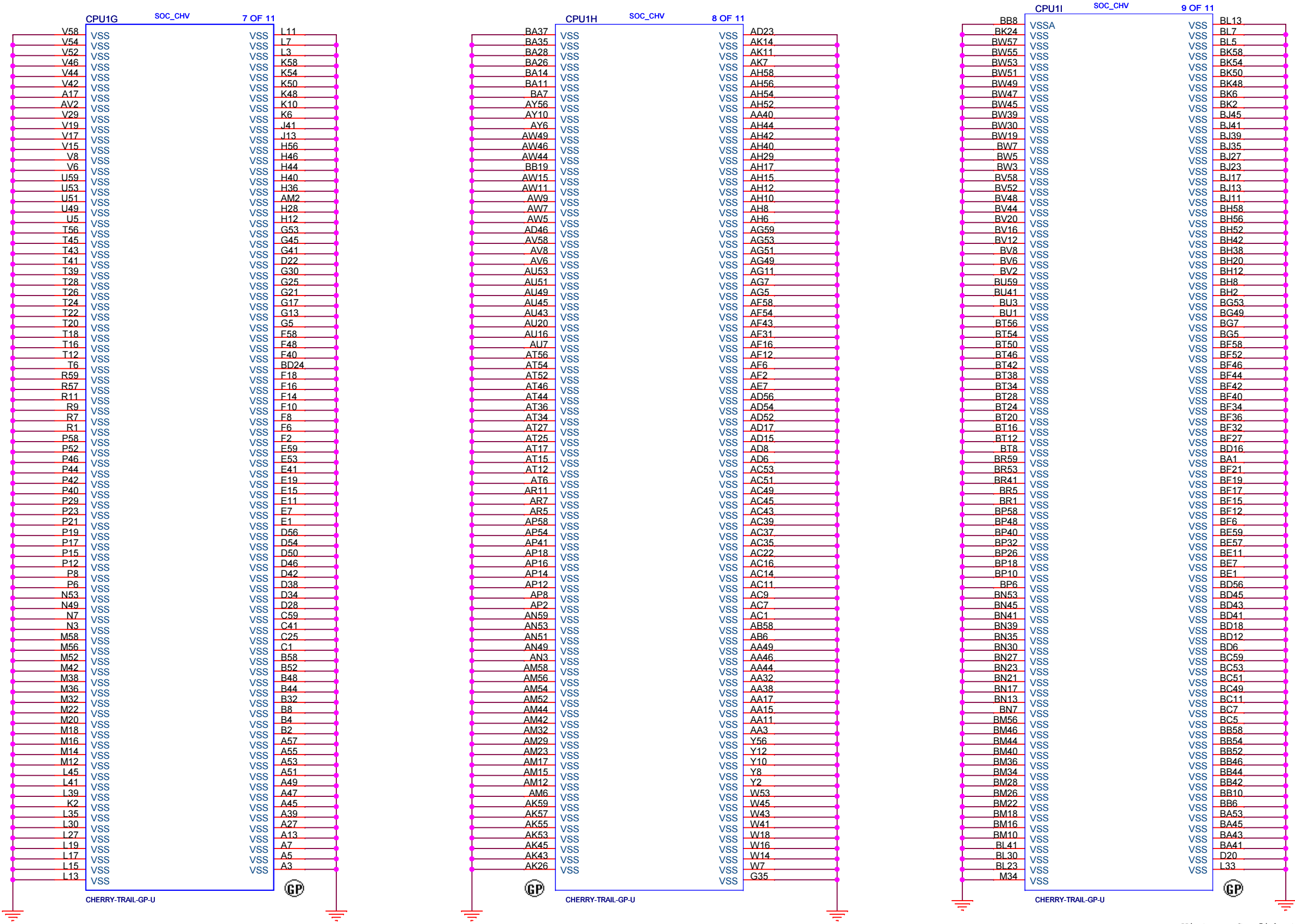
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Title <b>09_SOC (VCC/VNN)</b>			
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SOC : GROUND

20130923 modify



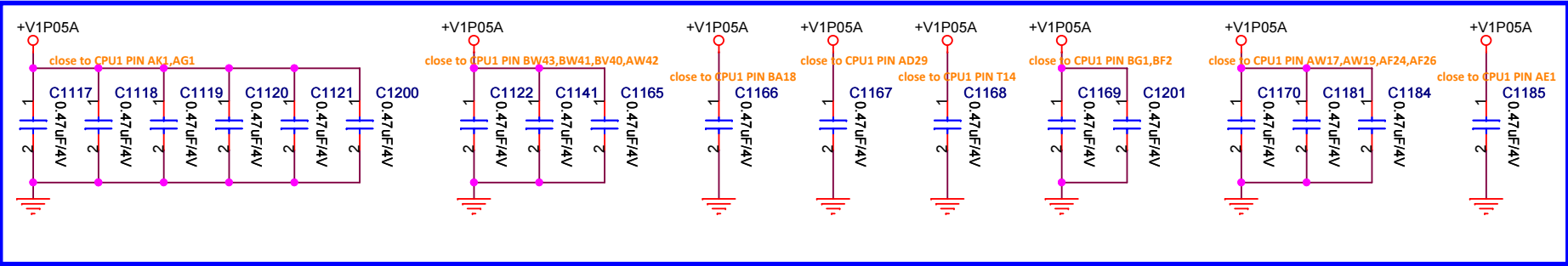
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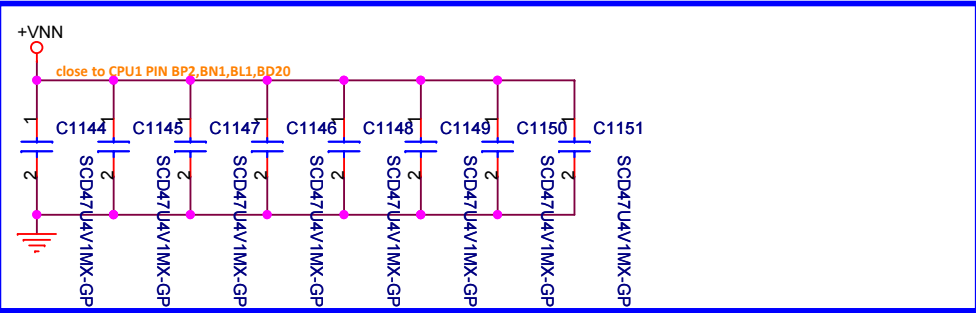
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>10_SOC (VSS)</b>			
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# SOC DECOUPLING

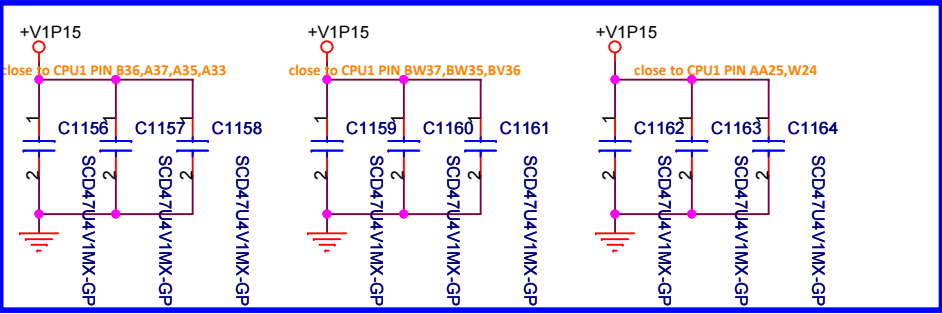
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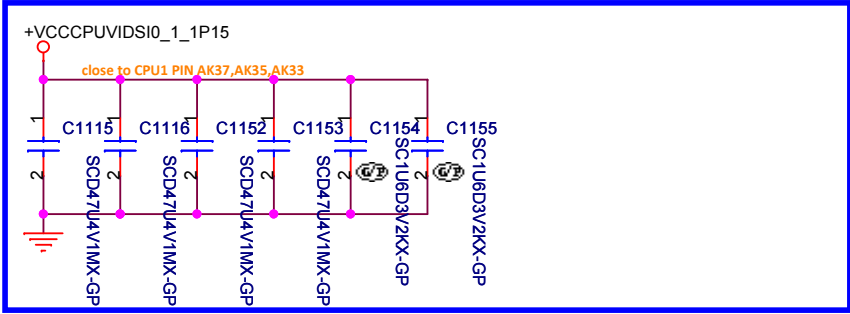
## +VNN



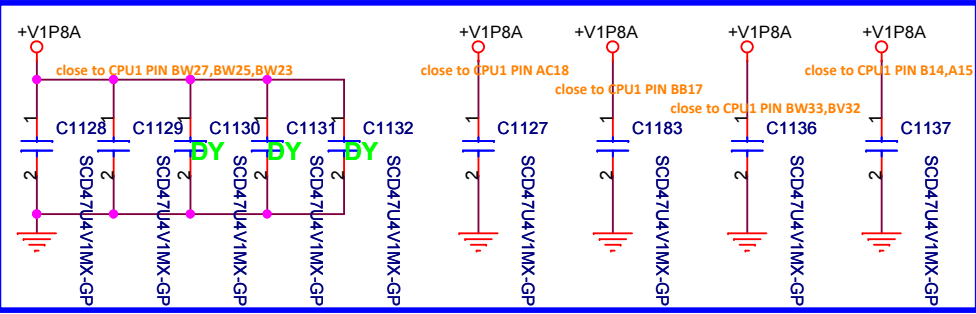
## +V1P15



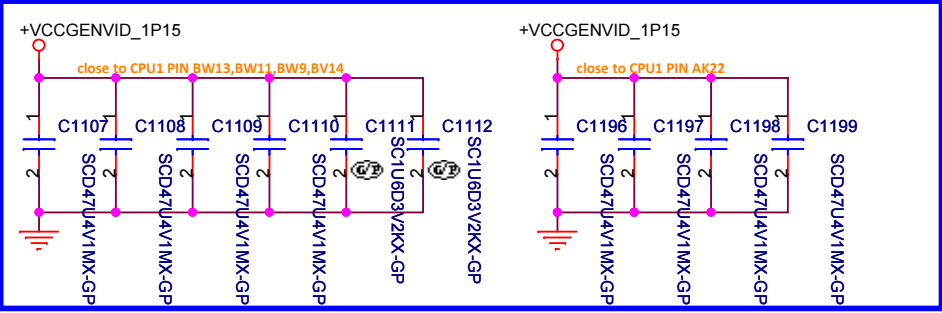
## +VCC1\_CPU



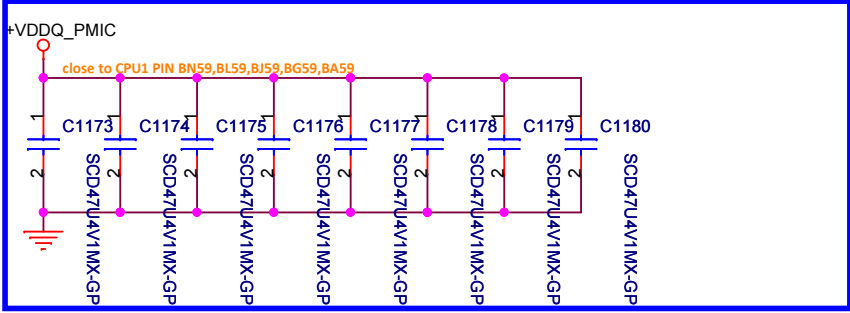
## +V1P8A



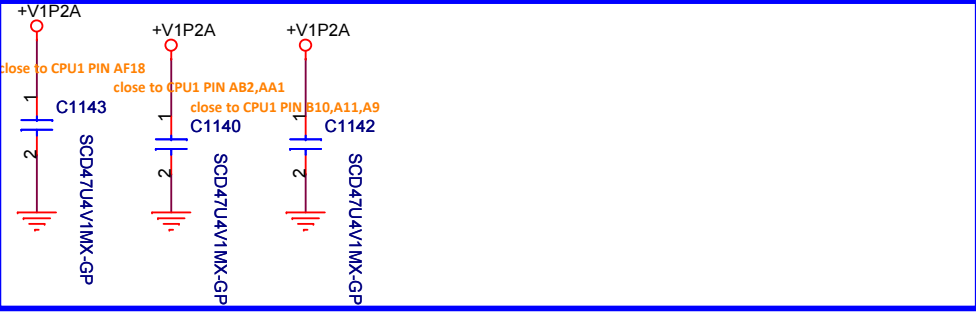
## +VGG



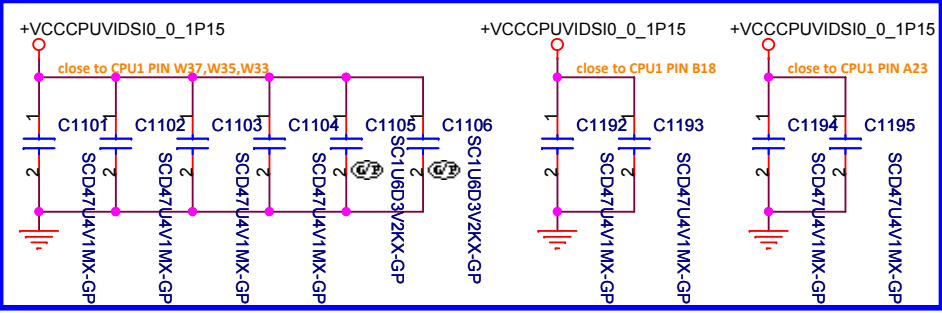
## +VDDQ\_PMIC



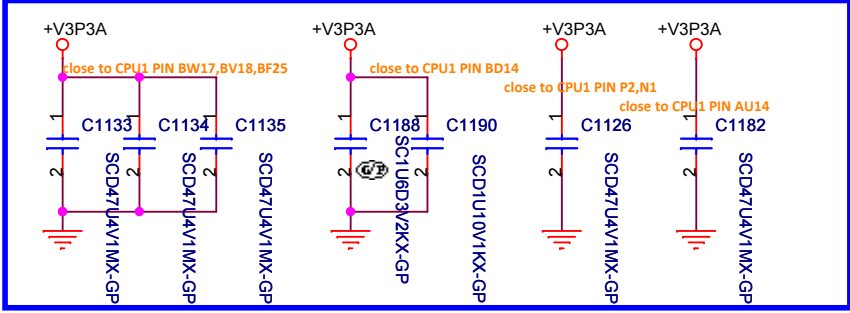
## +V1P2A



## +VCC0\_CPU



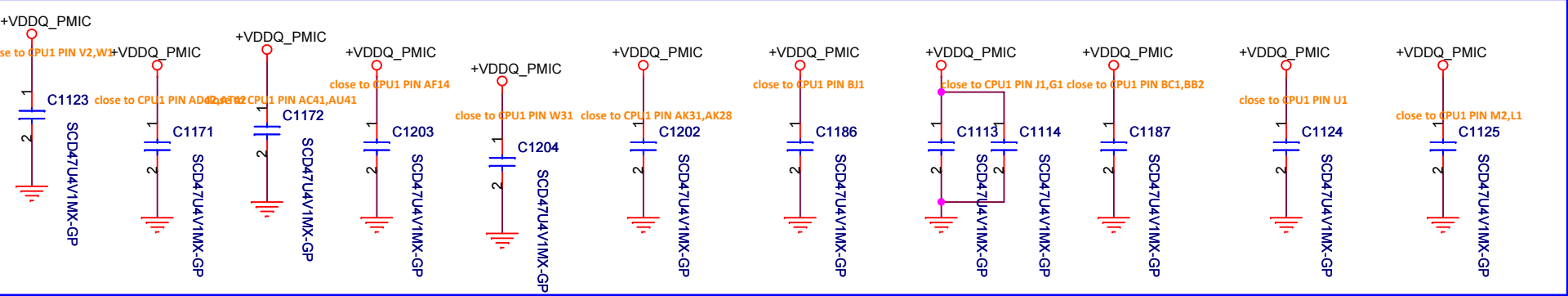
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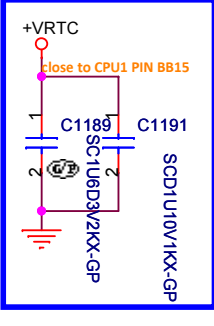
## +VSDIO



## +VDDQ\_PMIC



## +VRTC



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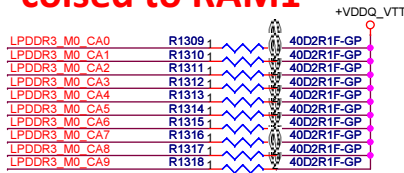
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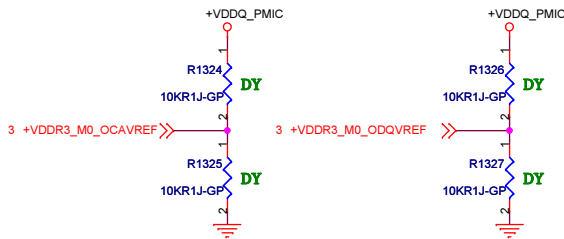
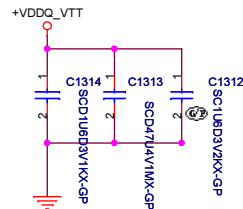


LPDDR3 MEMORY CHANNEL A  
K3QF2F20EM-AGCE-GP

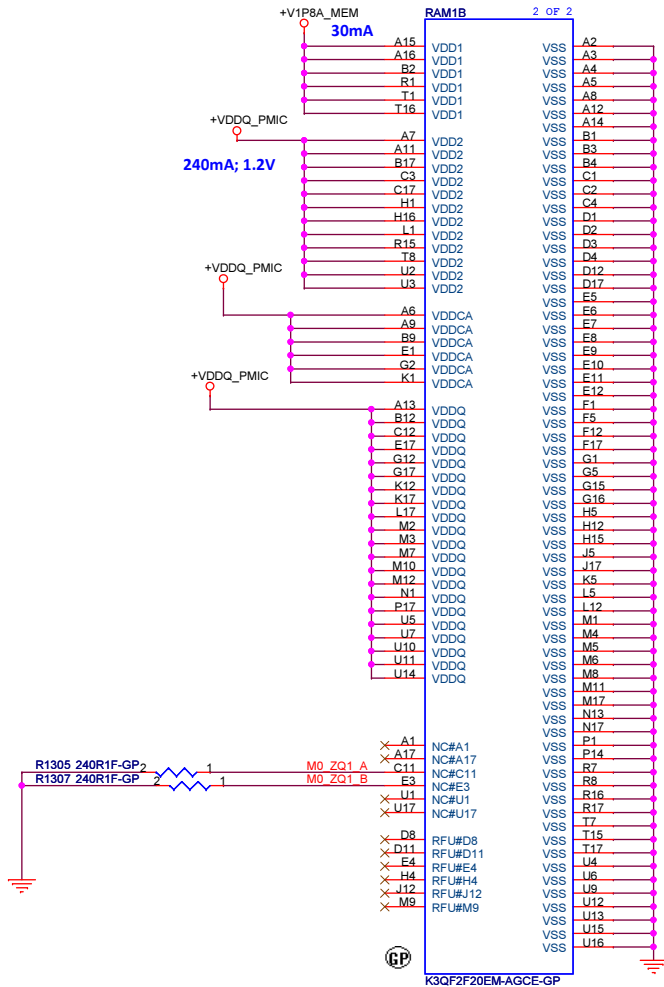
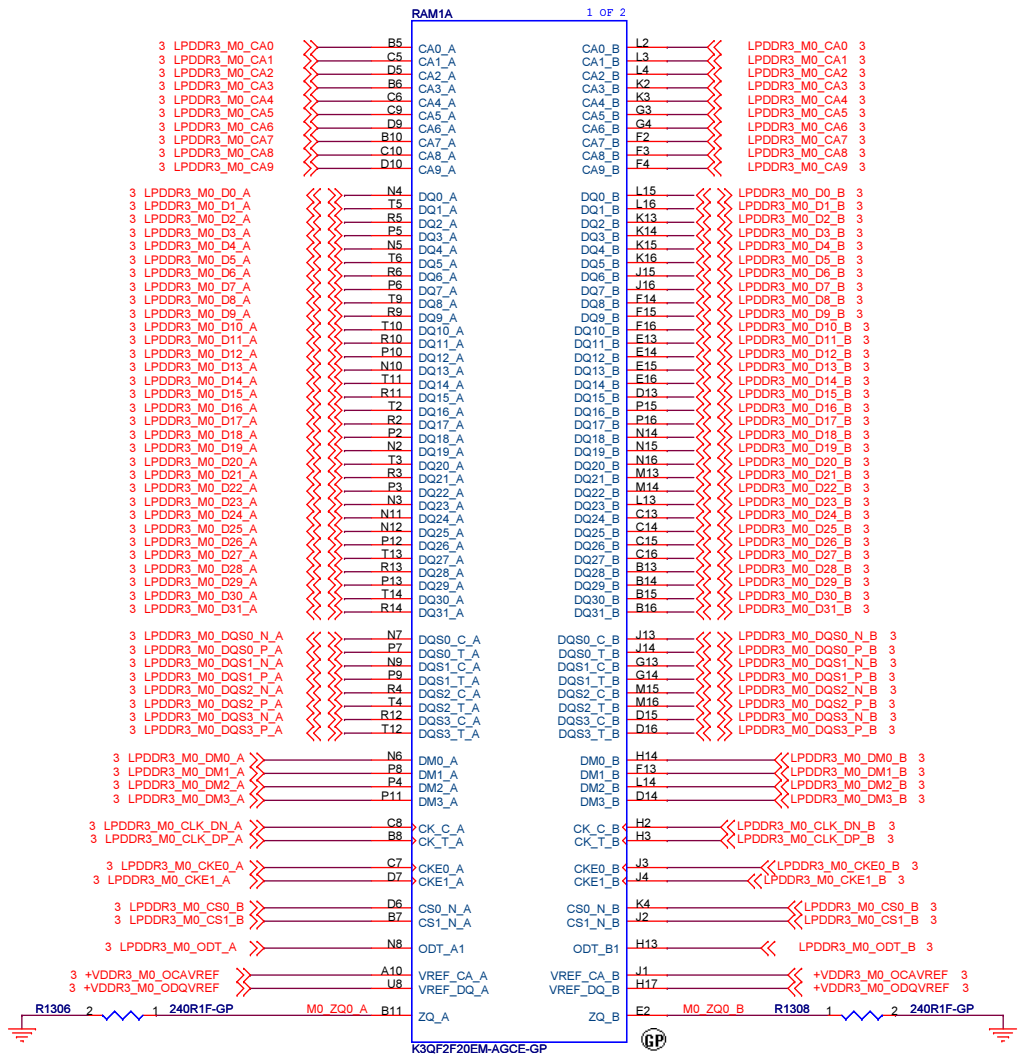
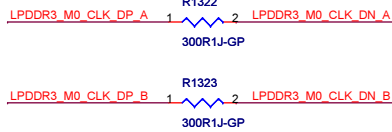
for layout:  
colsed to RAM1



LPDDR3 CA TERMINATION



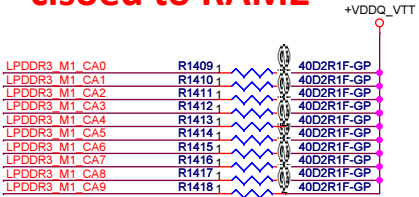
LPDDR3 CLK TERMINATION  
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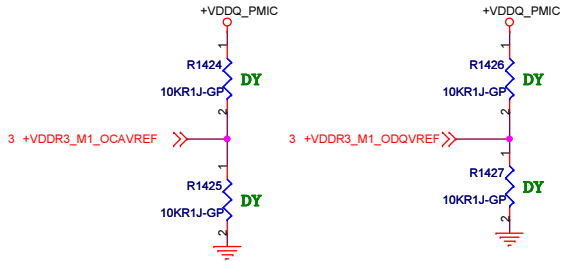
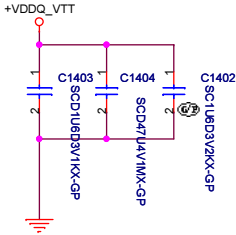
Somerset

LPDDR3 MEMORY CHANNEL B  
K3QF2F20EM-AGCE-GP

for layout:  
clsloed to RAM2

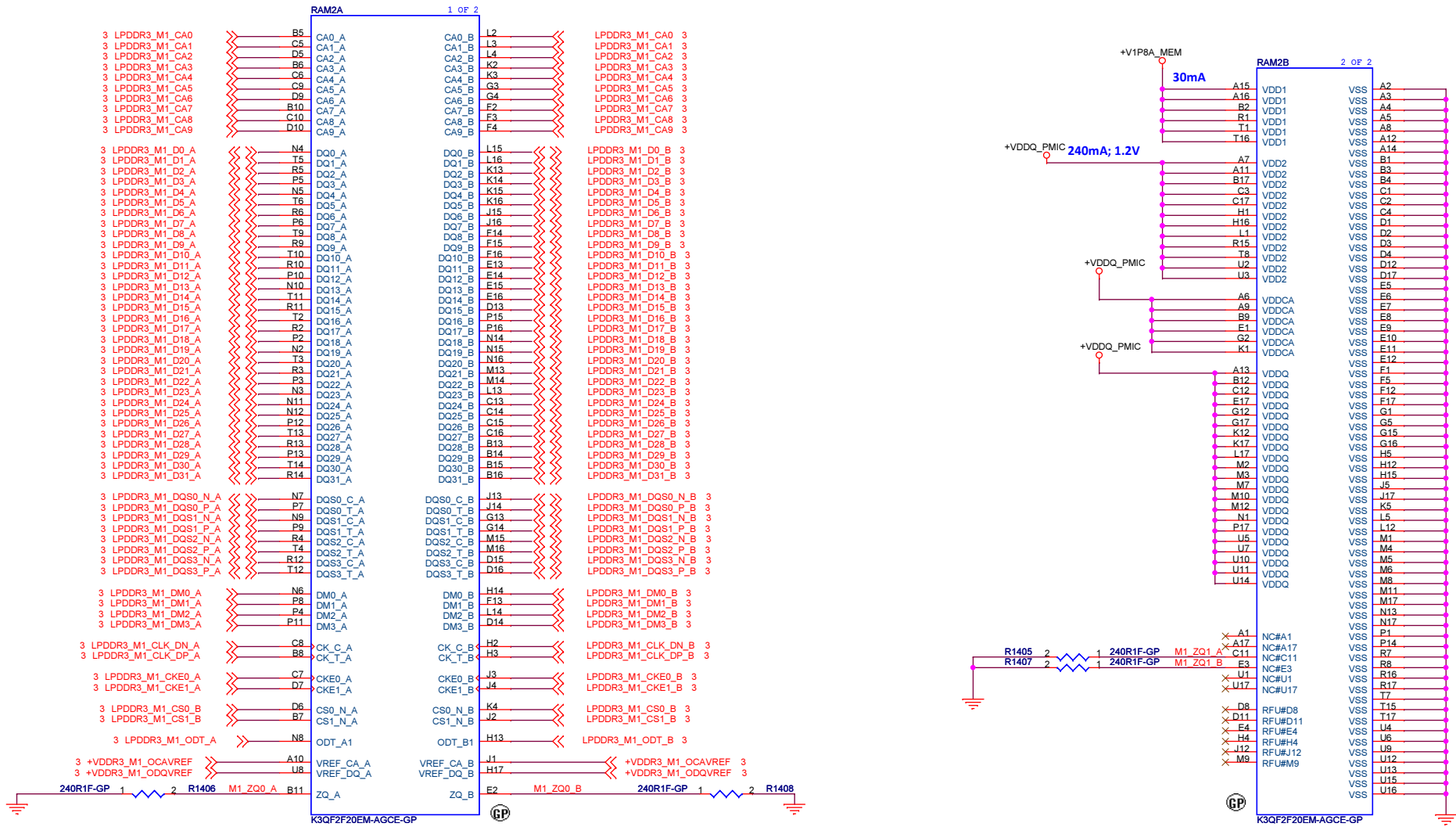
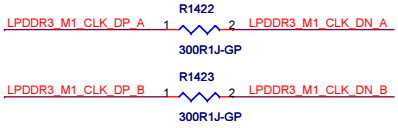


LPDDR3 CA TERMINATION



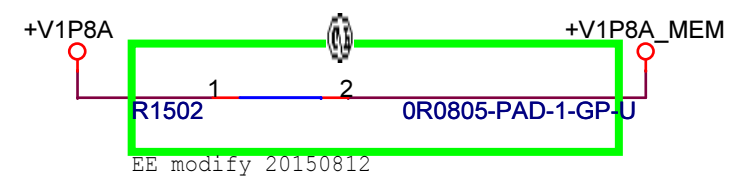
LPDDR3 CLK TERMINATION

for layout:close to RAM2



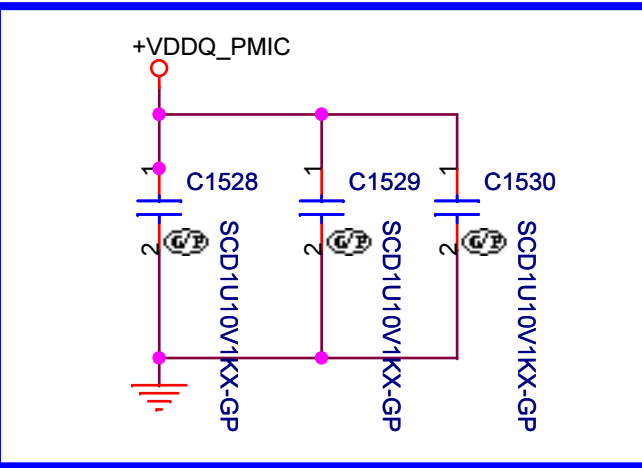
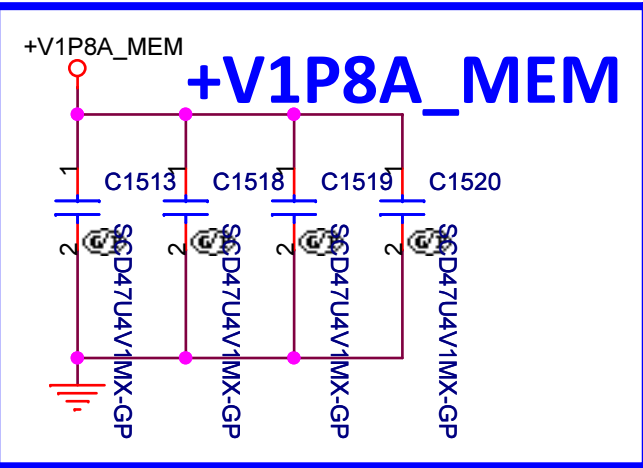
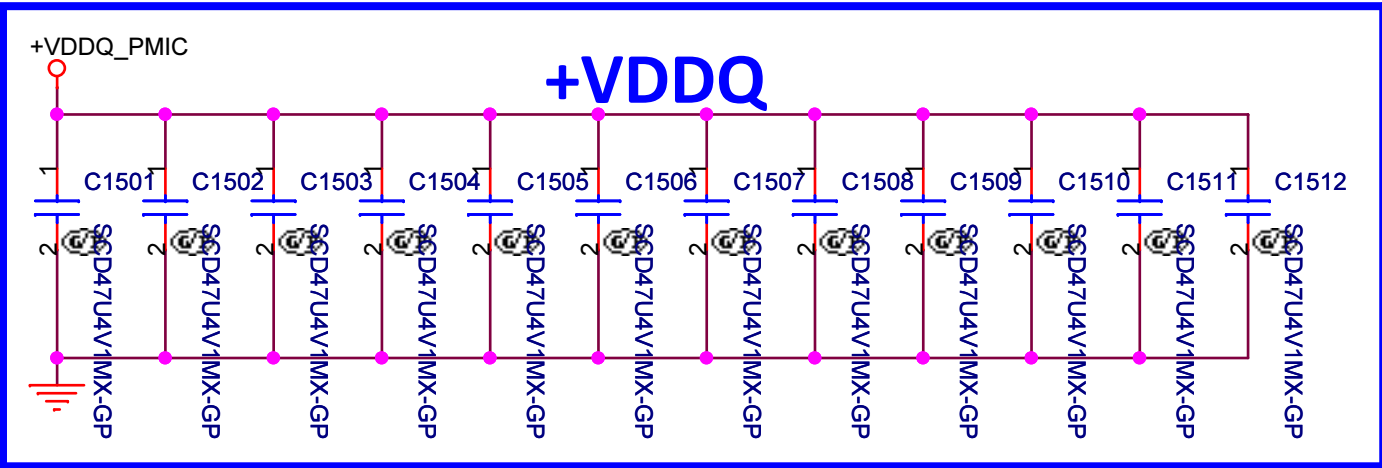
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LPDDR3 DECOUPLING CAPACITORS



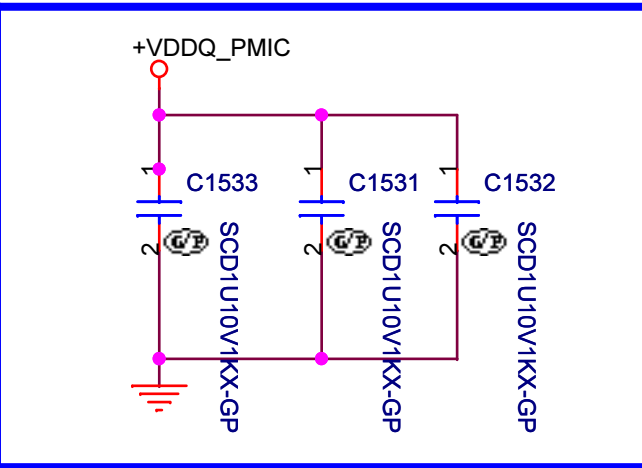
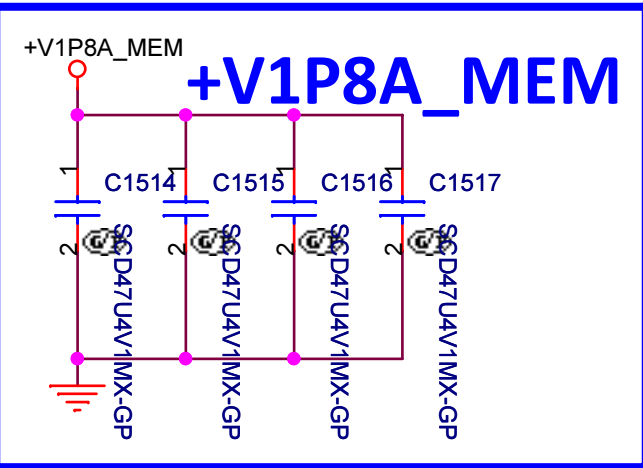
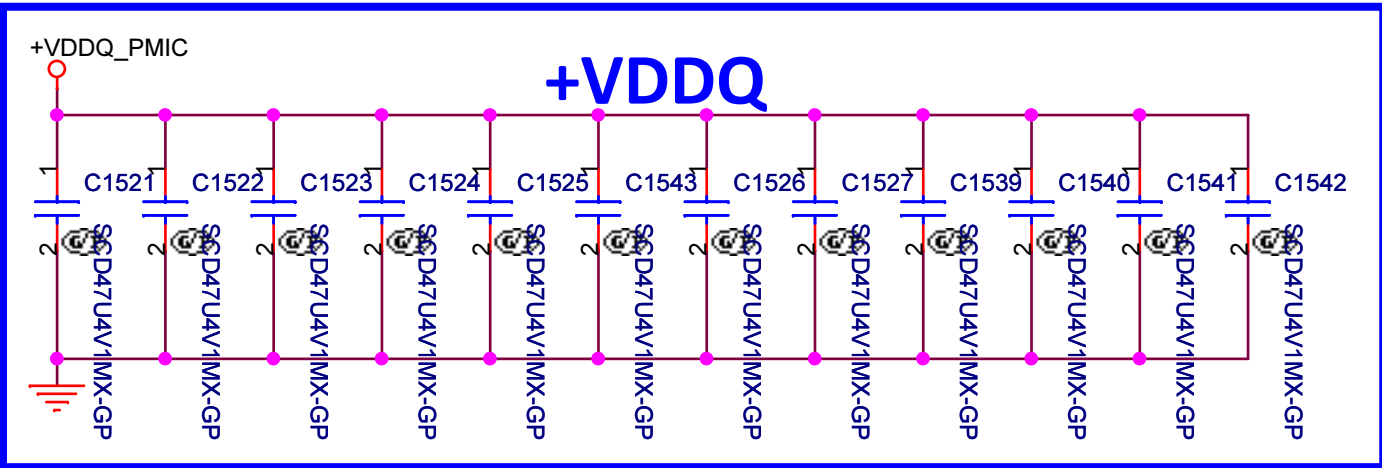
LPDDR3 MEMORY CHANNEL A

STITCHING CAPS



LPDDR3 MEMORY CHANNEL B

STITCHING CAPS



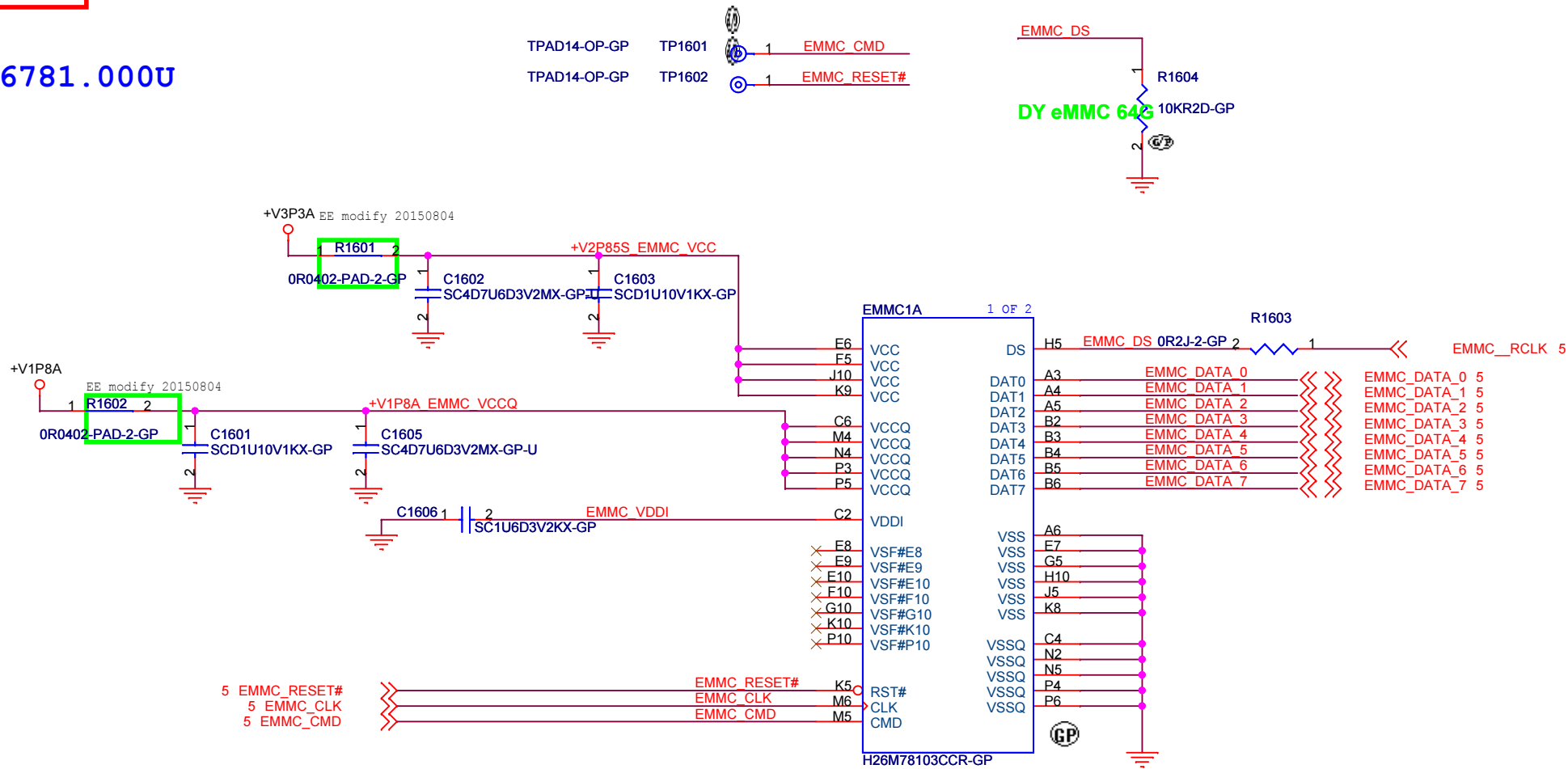
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15_LPDDR3_TERMINATIONS			
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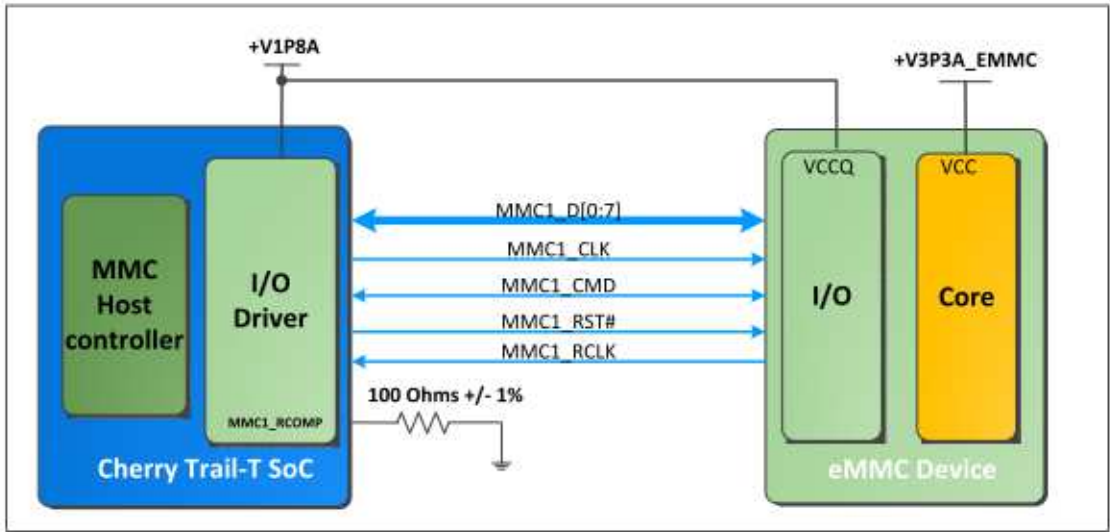
eMMC

64GB  
072.26781.000U



EMMC1B 2 OF 2			
A1	NC#A1	NC#J1	J1
A2	NC#A2	NC#J2	J2
A8	NC#A8	NC#J3	J3
A9	NC#A9	NC#J12	J12
A10	NC#A10	NC#J13	J13
A11	NC#A11	NC#J14	J14
A12	NC#A12	NC#K1	K1
A13	NC#A13	NC#K2	K2
A14	NC#A14	NC#K3	K3
B1	NC#B1	NC#K12	K12
B7	NC#B7	NC#K13	K13
B8	NC#B8	NC#K14	K14
B9	NC#B9	NC#L1	L1
B10	NC#B10	NC#L2	L2
B11	NC#B11	NC#L3	L3
B12	NC#B12	NC#L12	L12
B13	NC#B13	NC#L13	L13
B14	NC#B14	NC#L14	L14
C1	NC#C1	NC#M1	M1
C3	NC#C3	NC#M2	M2
C5	NC#C5	NC#M3	M3
C7	NC#C7	NC#M7	M7
C8	NC#C8	NC#M8	M8
C9	NC#C9	NC#M9	M9
C10	NC#C10	NC#M10	M10
C11	NC#C11	NC#M11	M11
C12	NC#C12	NC#M12	M12
C13	NC#C13	NC#M13	M13
C14	NC#C14	NC#M14	M14
D1	NC#D1	NC#N1	N1
D2	NC#D2	NC#N3	N3
D3	NC#D3	NC#N6	N6
D4	NC#D4	NC#N7	N7
D12	NC#D12	NC#N8	N8
D13	NC#D13	NC#N9	N9
D14	NC#D14	NC#N10	N10
E1	NC#E1	NC#N11	N11
E2	NC#E2	NC#N12	N12
E3	NC#E3	NC#N13	N13
E12	NC#E12	NC#N14	N14
E13	NC#E13	NC#P1	P1
E14	NC#E14	NC#P2	P2
F1	NC#F1	NC#P7	P7
F2	NC#F2	NC#P8	P8
F3	NC#F3	NC#P9	P9
F12	NC#F12	NC#P11	P11
F13	NC#F13	NC#P12	P12
F14	NC#F14	NC#P13	P13
G1	NC#G1	NC#P14	P14
G2	NC#G2		
G12	NC#G12		
G13	NC#G13	RFU#A7	A7
G14	NC#G14	RFU#E5	E5
H1	NC#H1	RFU#G3	G3
H2	NC#H2	RFU#K6	K6
H3	NC#H3	RFU#K7	K7
H12	NC#H12		
H13	NC#H13		
H14	NC#H14		

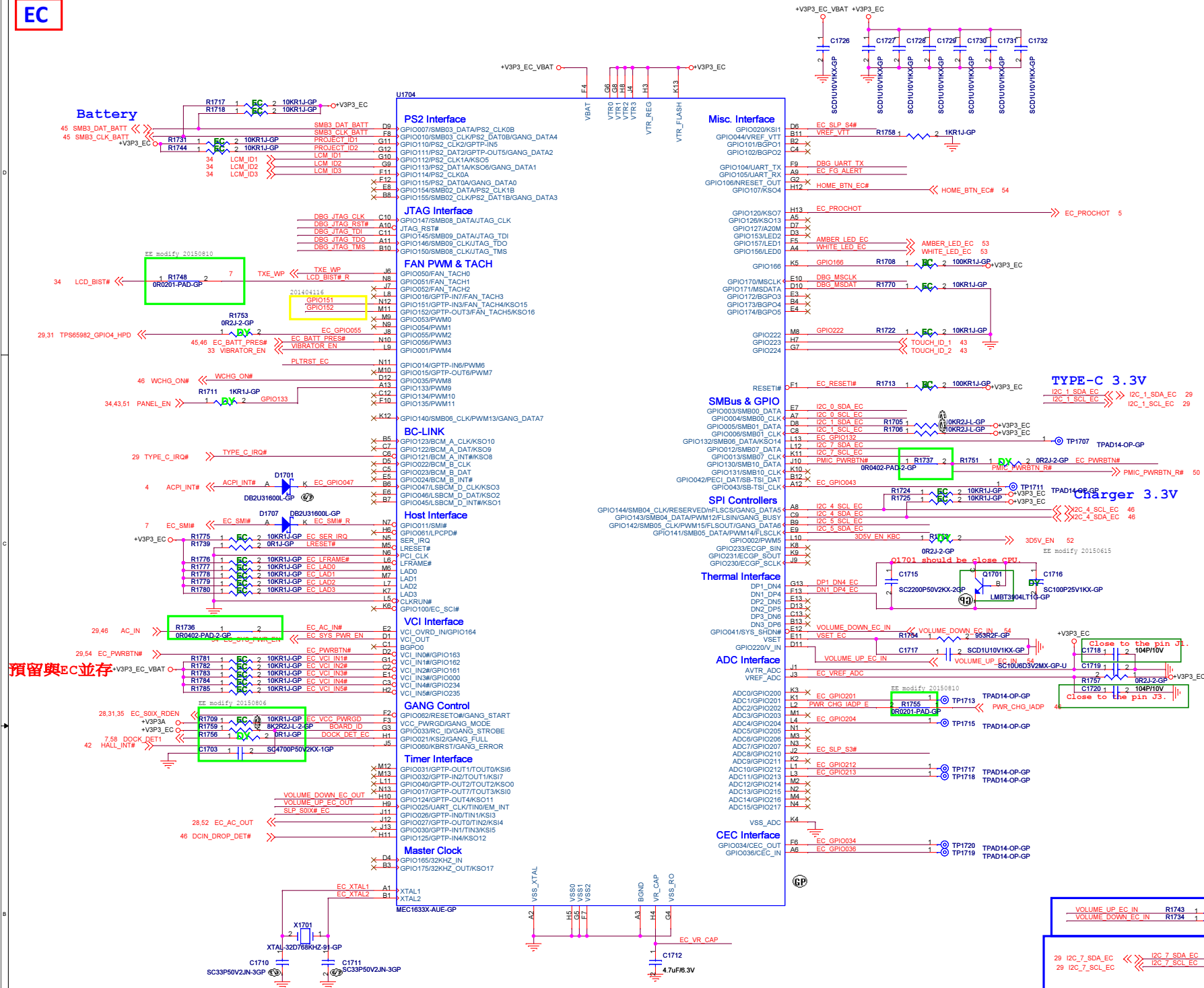
Figure 3-44.eMMC Interface Topology



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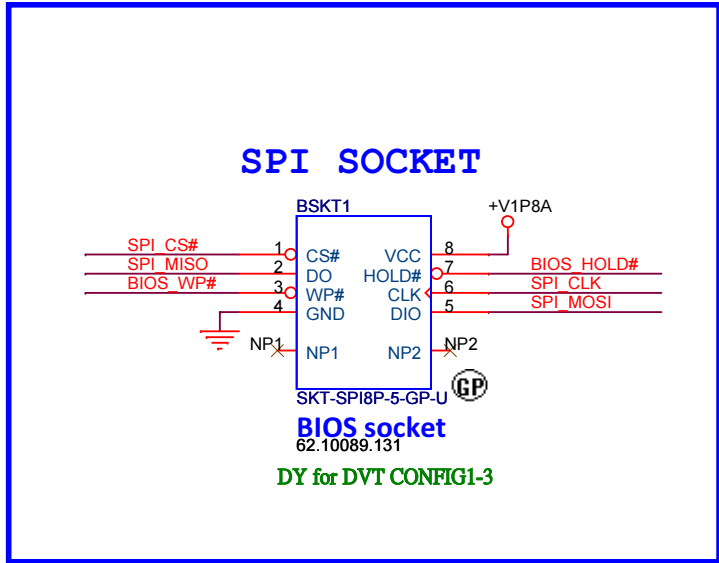
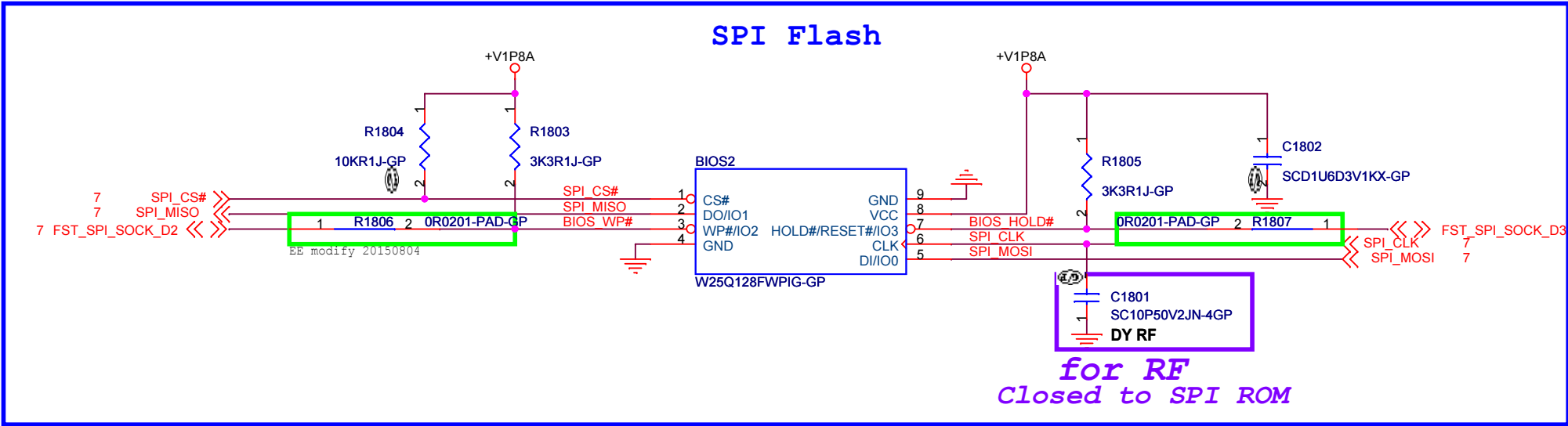




NFC			NFC_ID1	NFC_ID2
NON-NFC SKU			0	1
NFC SKU			1	1

BOARD ID			PROJECT ID		
REV	R	C	PROJECT	PROJECT_ID2	PROJECT_ID1
EVT1	240K	4700p	Blackwell-T3	0	0
EVT2	130K	4700p	Blackwell-T4	0	1
DVT1	62K	4700p	Somerset-T3	1	0
DVT2	33K	4700p	Somerset-T4	1	1
PVT1	8.2K	4700p			
MP	4.3K	4700p			
	2K	4700p			
	1K	4700p			

SPI ROM




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Thermal Protect

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Size	Document Number <b>Somerset</b>		Rev <b>SA</b>
Date:	Sunday, September 27, 2015		Sheet   19   of   72

# AUDIO CODEC

(AVDD+CPVDD+DBVDD) 1.8V=200mA (max)  
(MICVDD) 3.3= 50mA (max)  
(SPKVDDL+R) 5V = 2A (max)

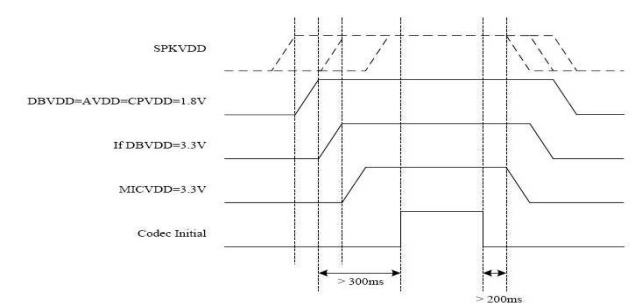
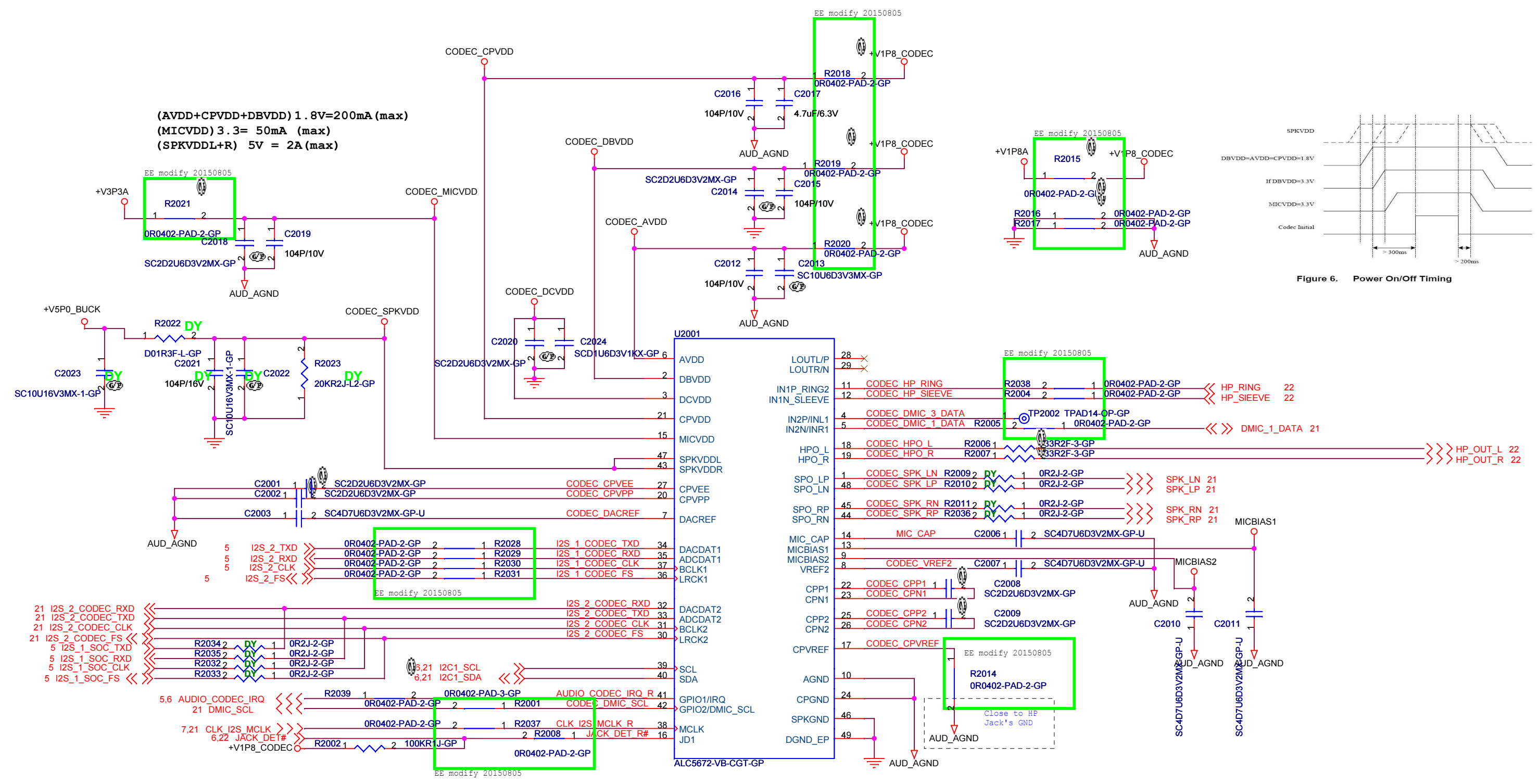
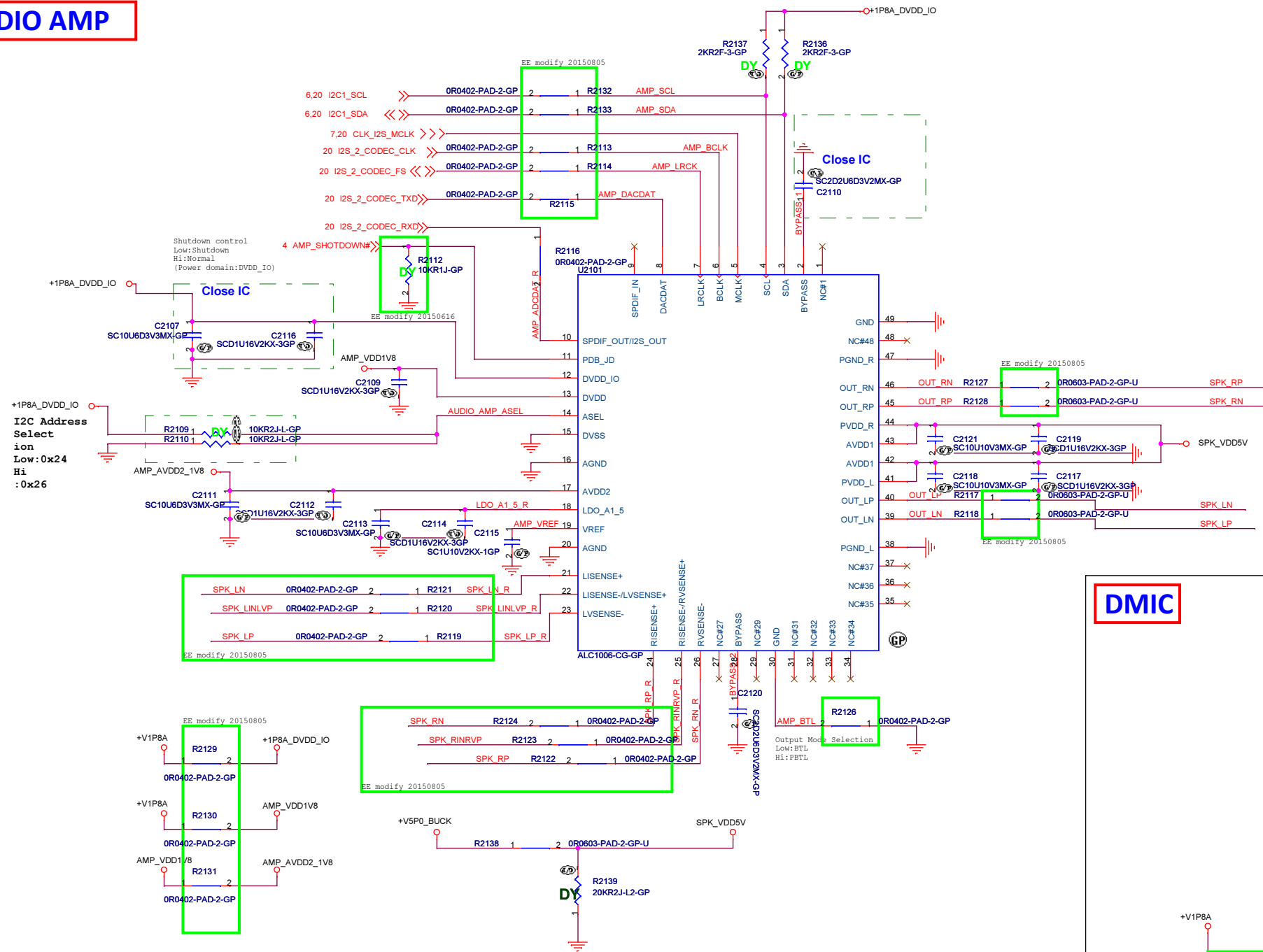


Figure 6. Power On/Off Timing

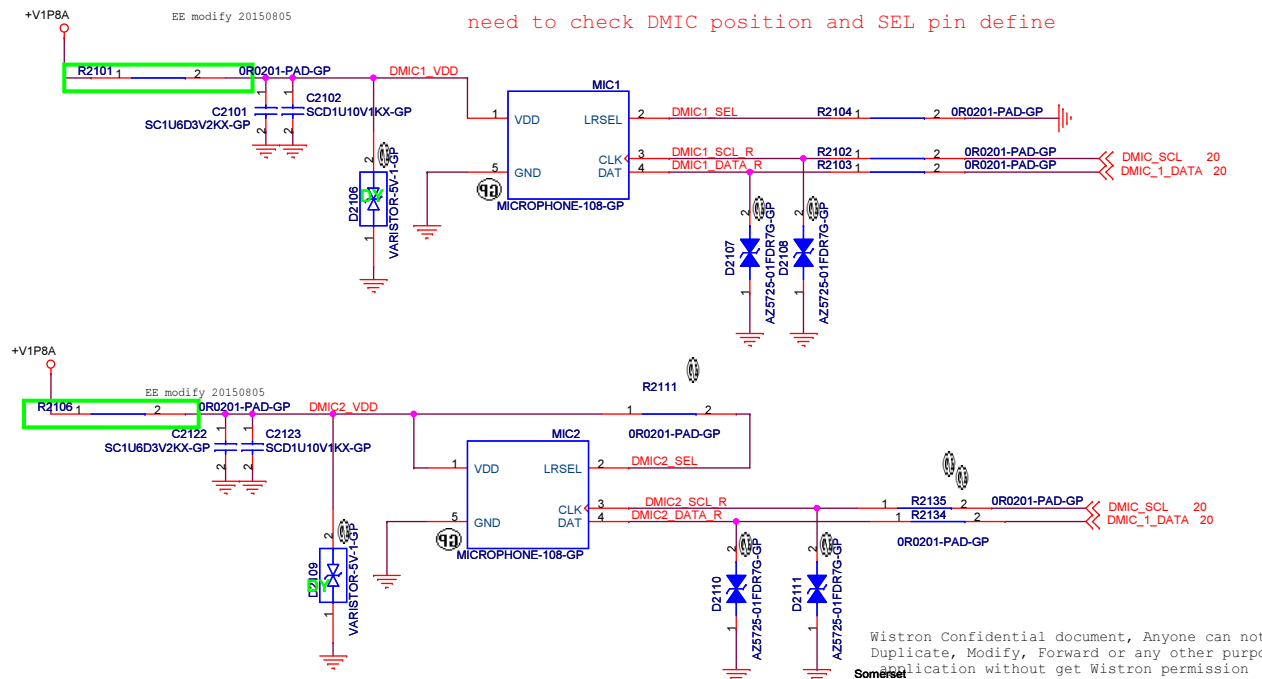
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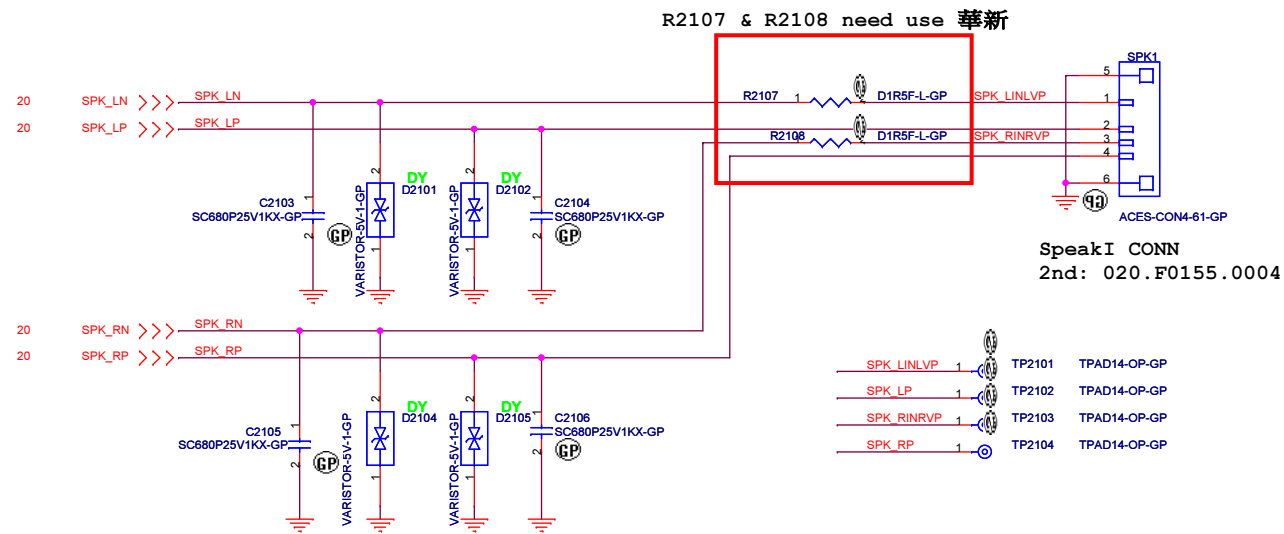
AUDIO AMP



DMIC

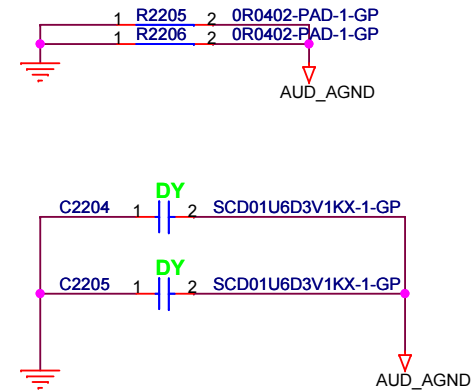
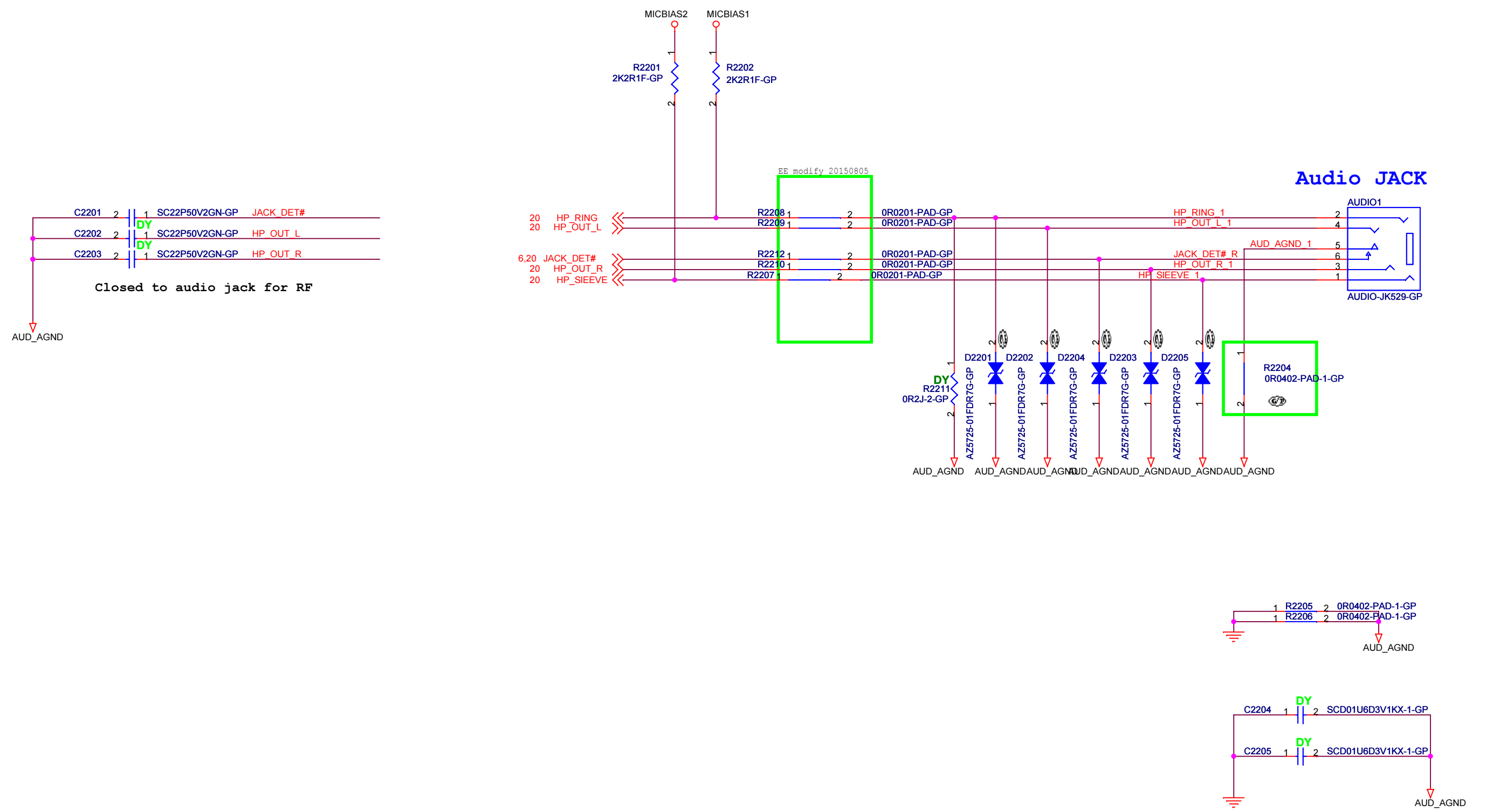


SPEAKER



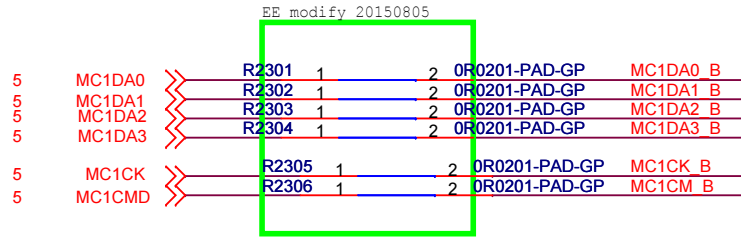
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Device :AUDIO JACK

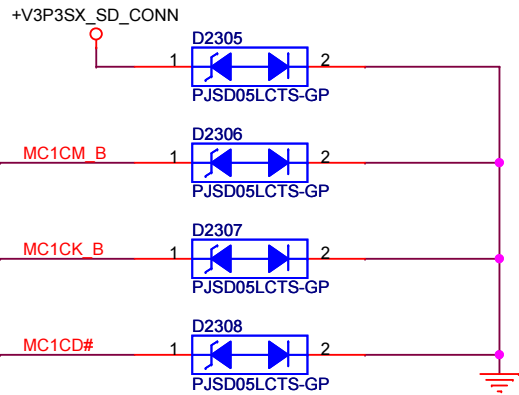
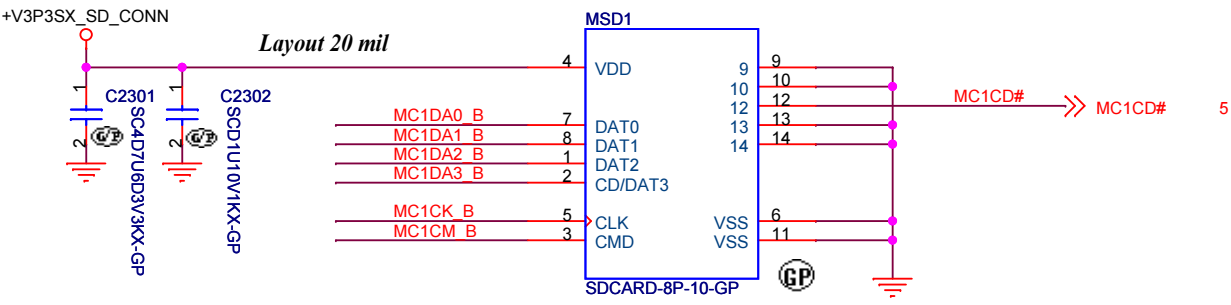
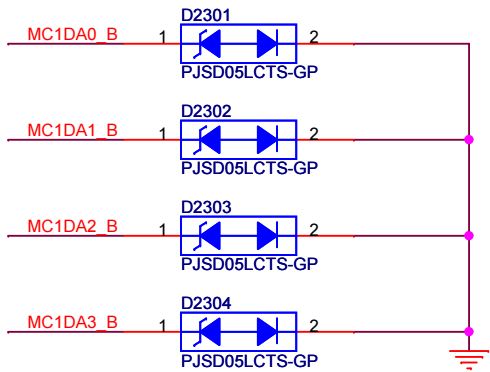


SD Controller

SD CARD

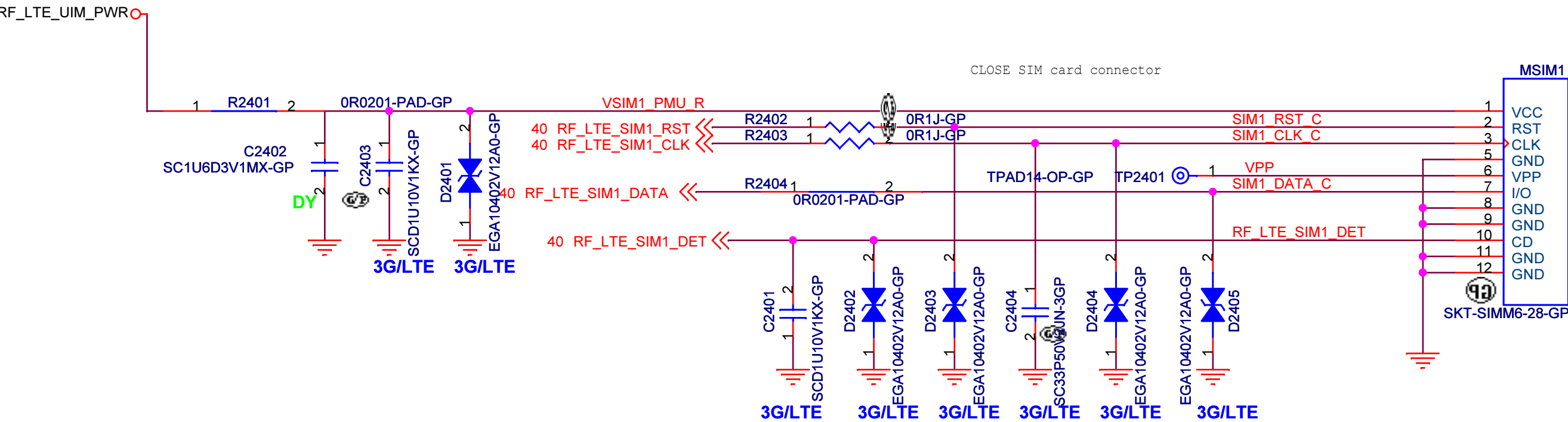


for ESD/RF Closed to SDC1



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SIM CARD



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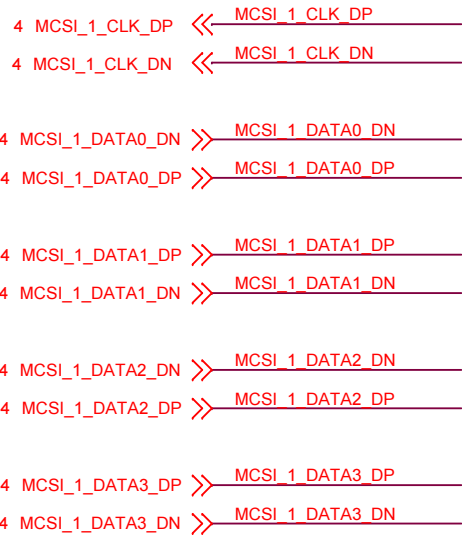
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Title			
24_uSIM CONN			
Size	Document Number		Rev
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Date:	Sunday, September 27, 2015	Sheet 24 of	72

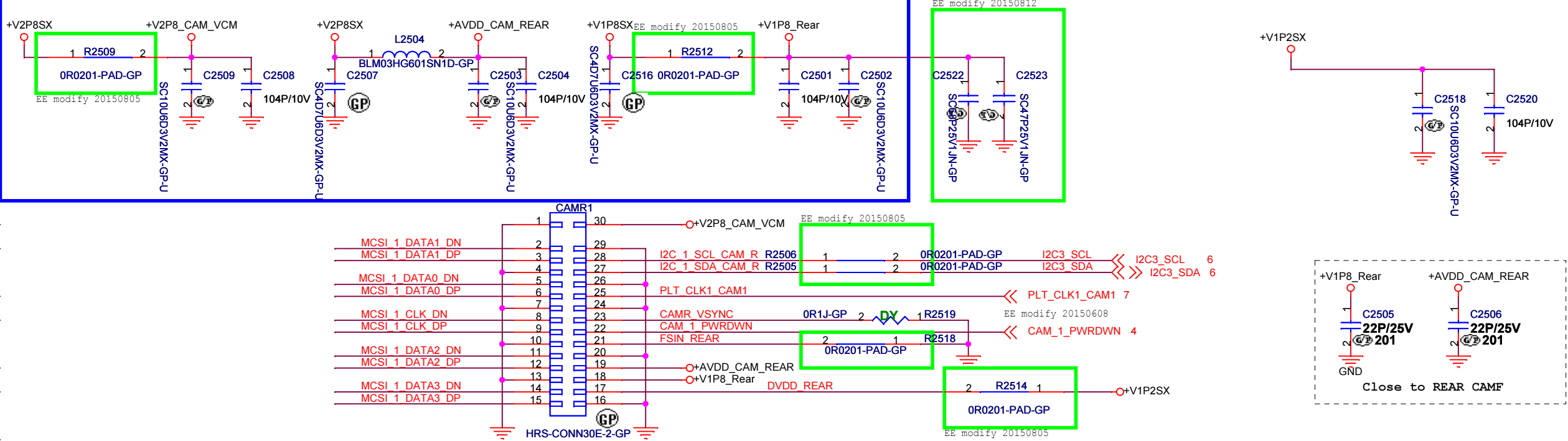


Rear Camera

Rear Camera  
OV08858-G04A(8M)  
P8V12F-203(8M)

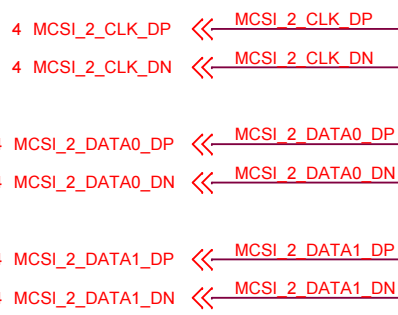


Rear Camera Power

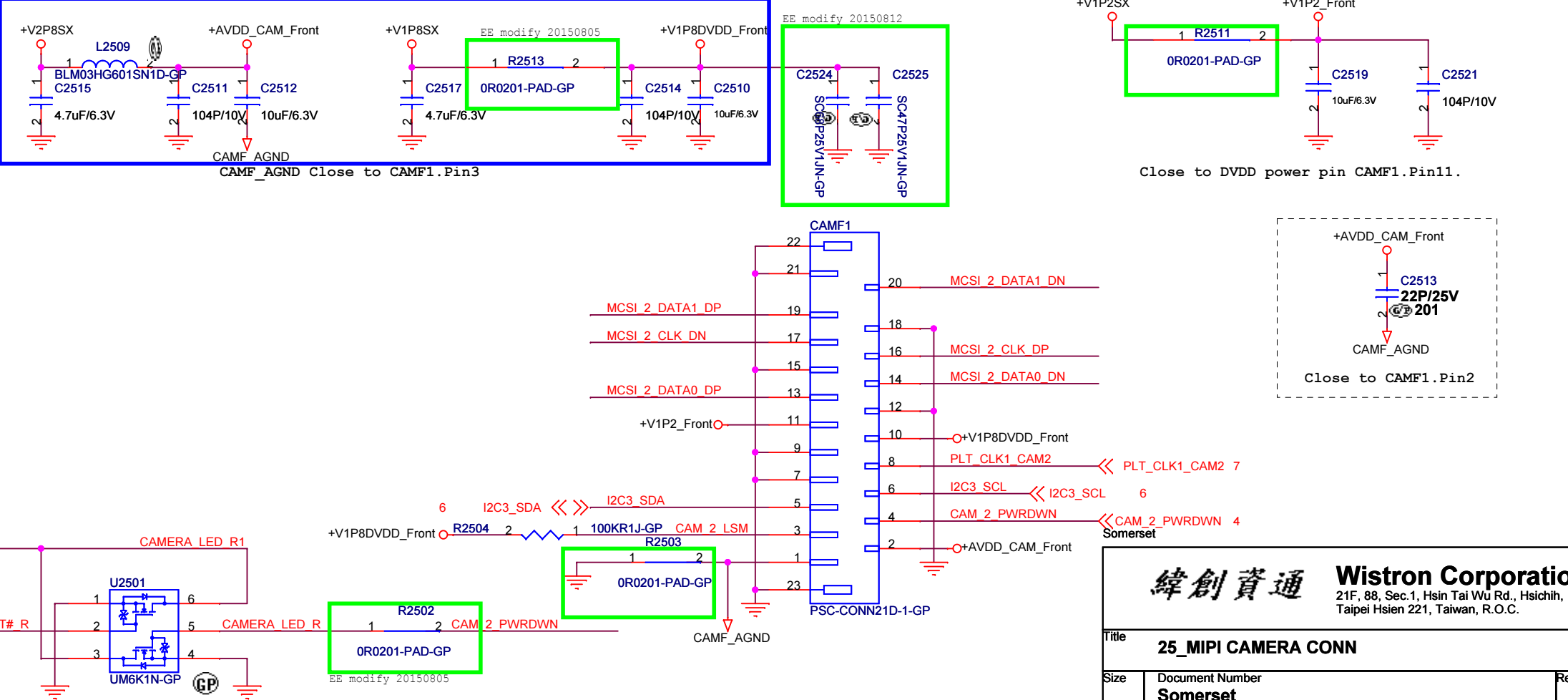


Front Camera

Front Camera  
OV2740(2M)  
need to check the connector & pin define



Front Camera Power



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Title 25\_MIPI CAMERA CONN

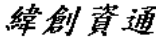
Size Document Number Somerset

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3D Camera


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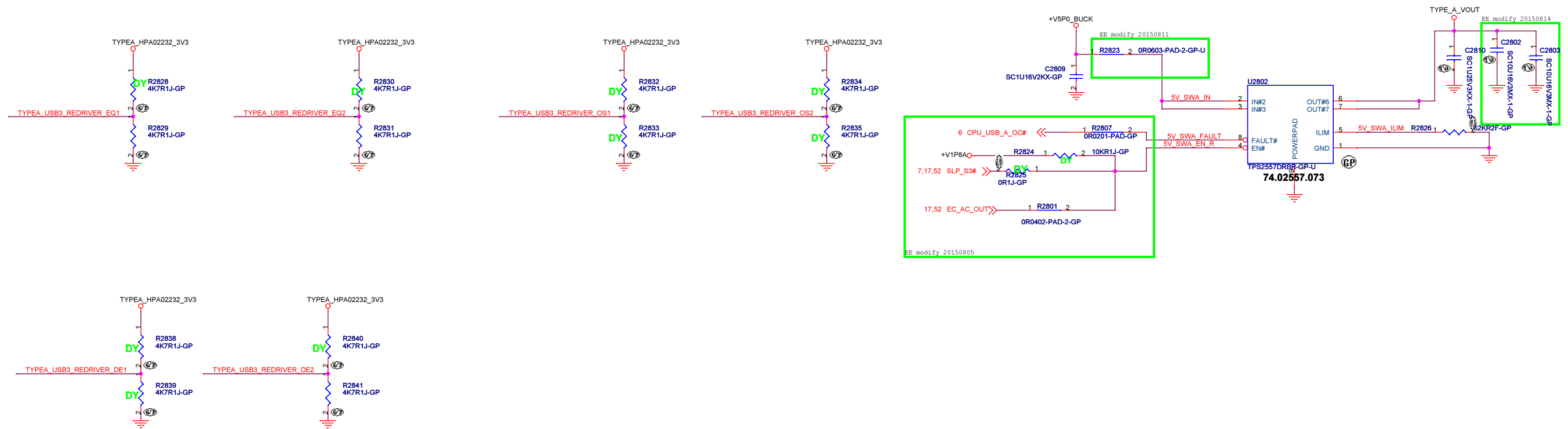
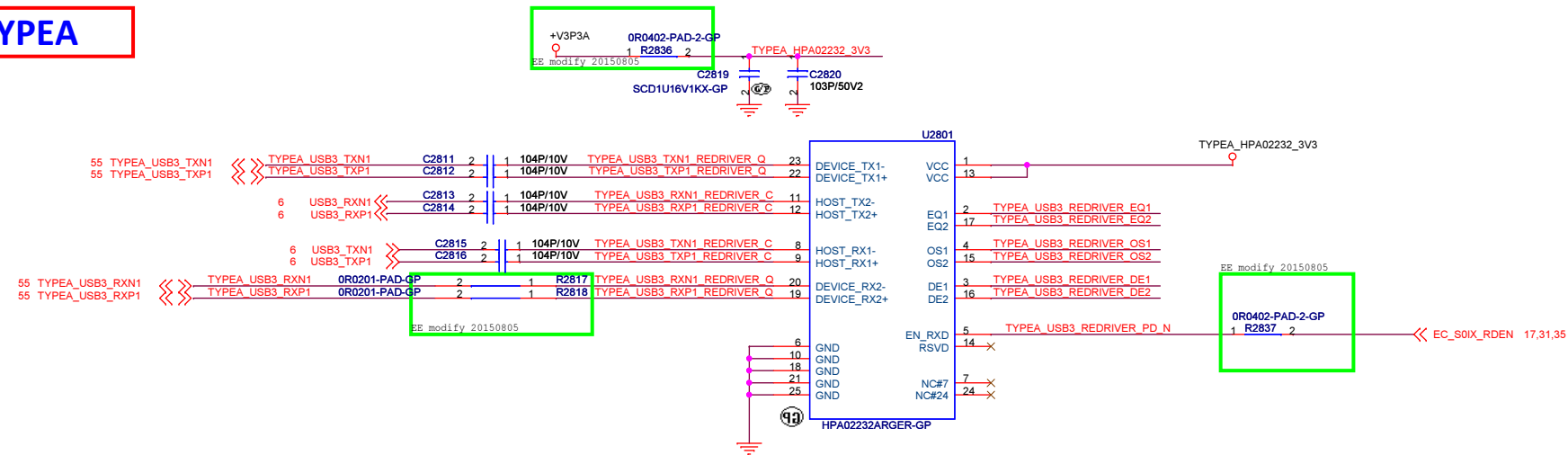
		<b>Wistron Corporation</b> <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title <b>26_Camera_3D</b>			
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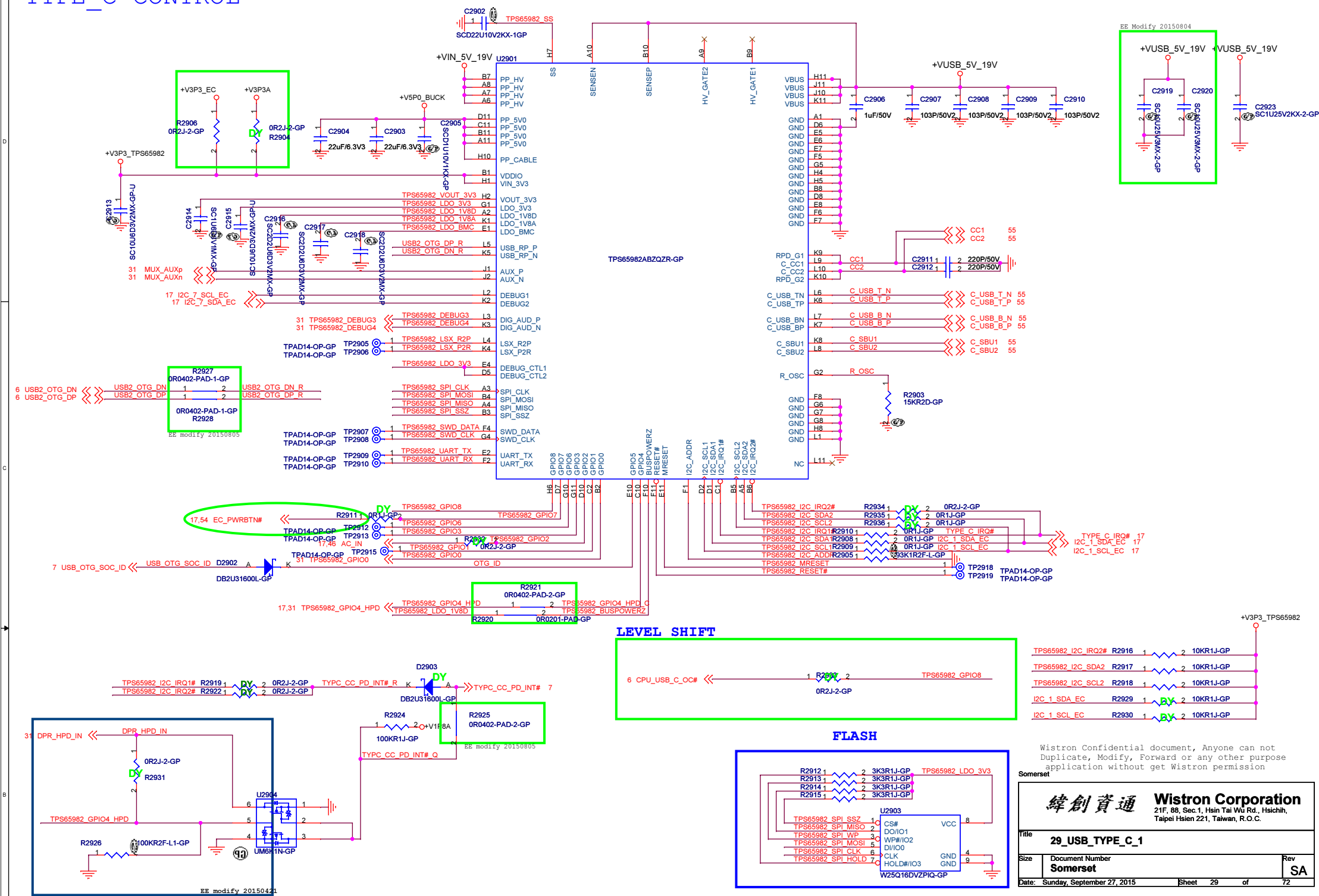
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Title <b>27_USBPHY/SW</b>			
Size	Document Number <b>Somerset</b>		Rev <b>SA</b>
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**TYPEA**




## TYPE\_C CONTROL



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Title <b>29_USB_TYPE_C_1</b>			
Size	Document Number <b>Somerset</b>		Rev <b>SA</b>
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Title <b>30_RESERVED_USB_TYPE_C_2</b>			
Size	Document Number <b>Somerset</b>		Rev <b>SA</b>
Date:	Sunday, September 27, 2015	Sheet 30 of	72

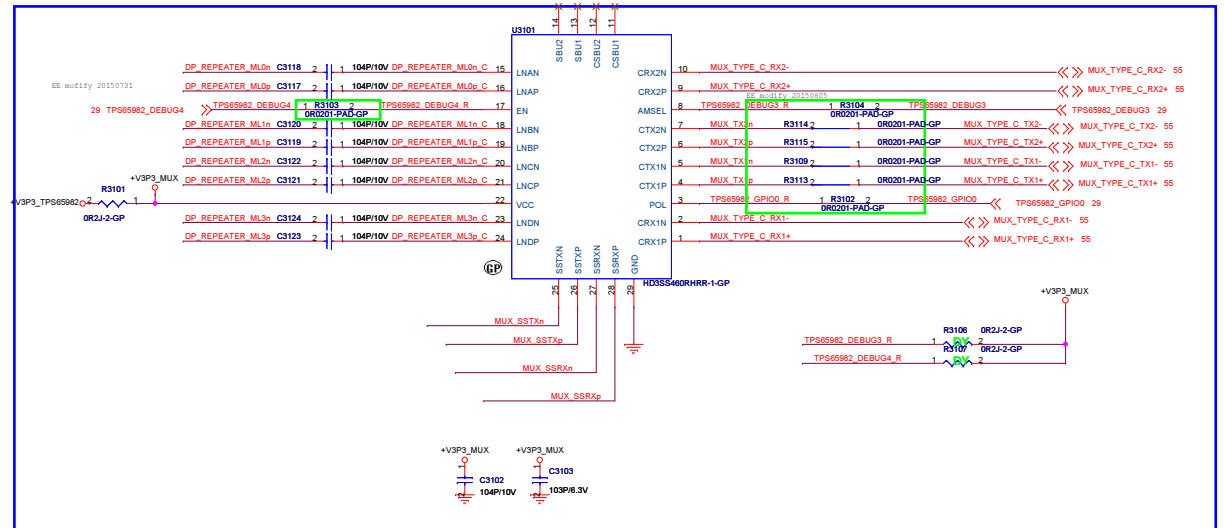
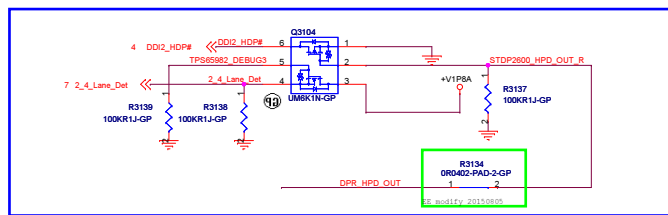
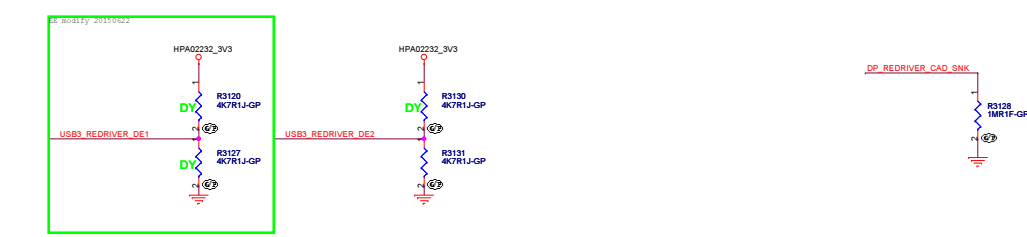
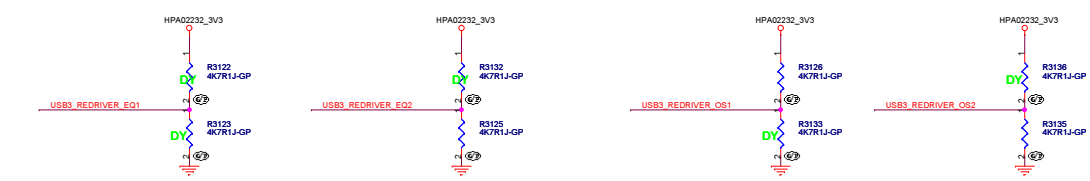
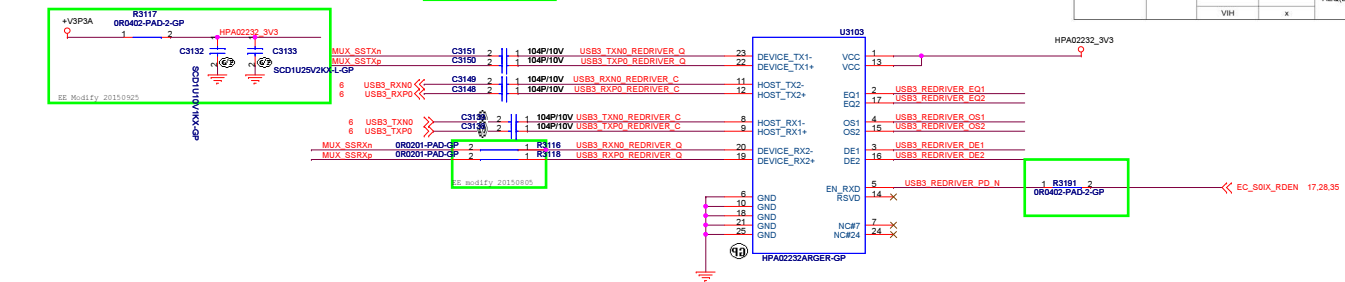
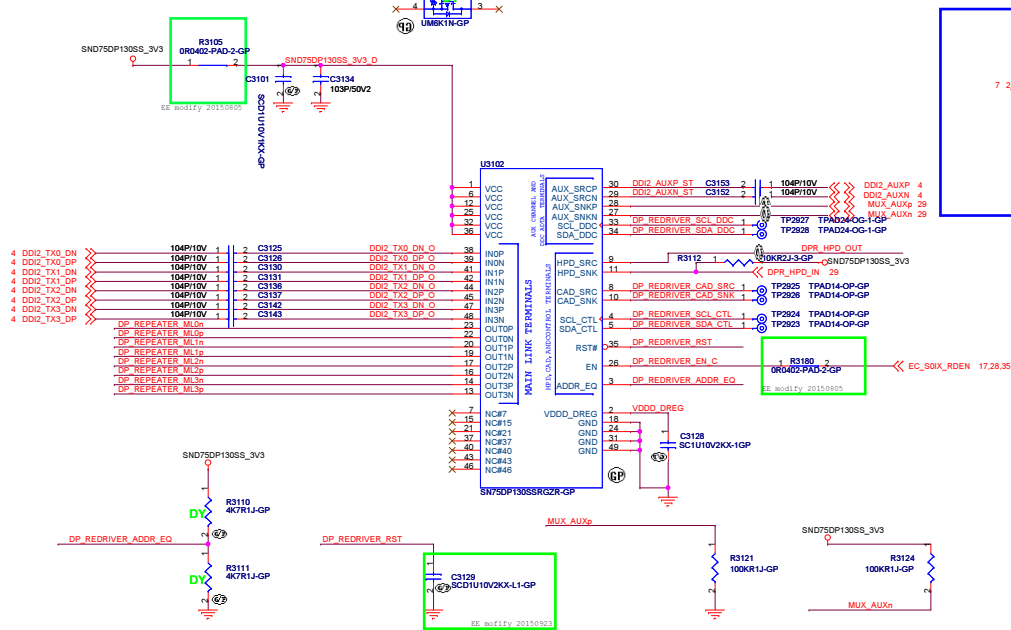
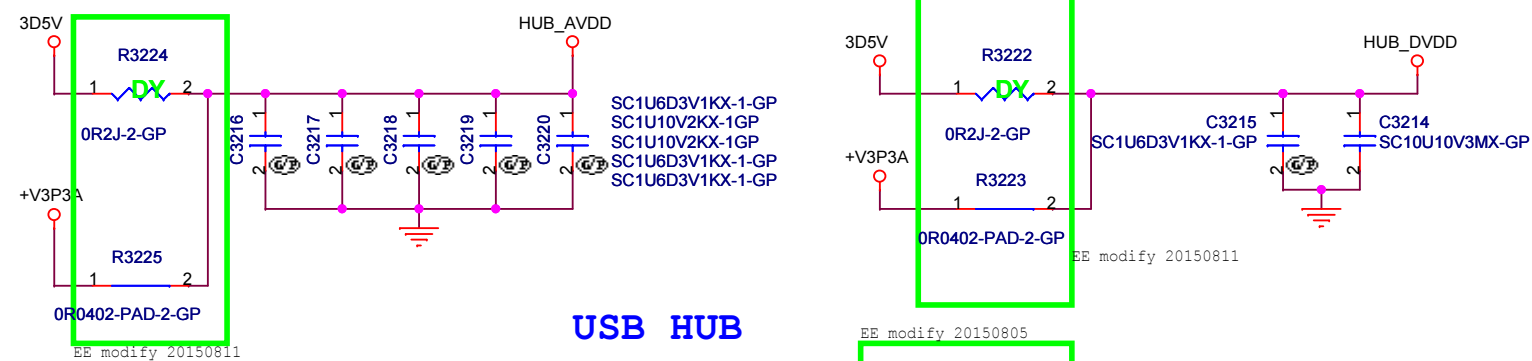


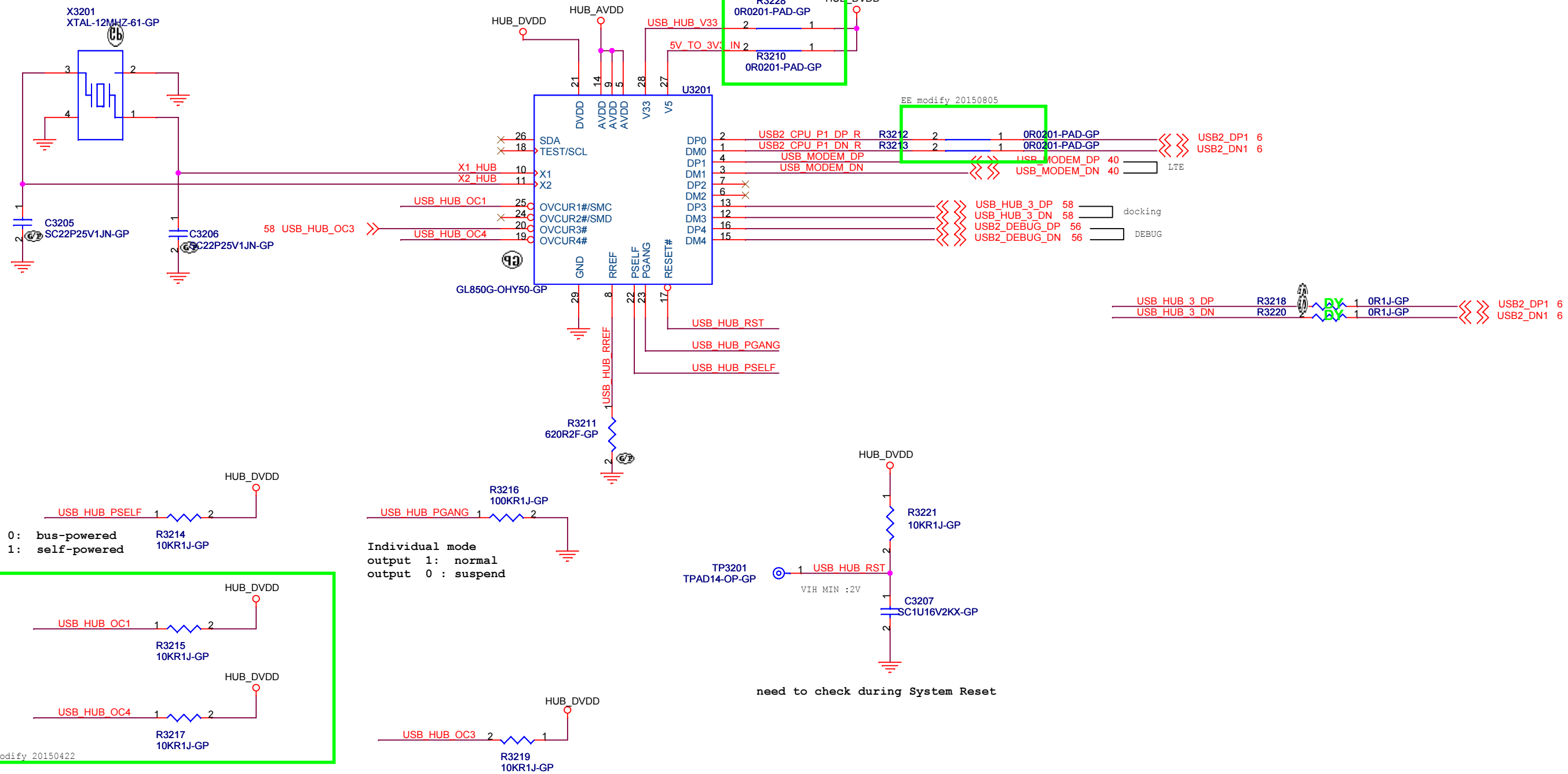
Table 2. Signal Control Pin Setting						DESCRIPTION
OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)						
OSx <sup>(1)</sup>	TRANSITION BIT AMPLITUDE (TYP mVpp)	EQx <sup>(1)</sup>	EQUALIZATION (dB)		low-range EQ gain in training; DP mode  mode: feed EQ  mode: feed EQ  mode: feed EQ	
NC (default)	1042	NC (default)	7			
1	908	0	0			
1	1127	1	15			
OUTPUT DE OF CONTROL (at 2.5 GHz)						high-range EQ gain in training; DP mode  mode: feed EQ  mode: feed EQ  mode: feed EQ  high-range EQ gain in training; DP mode  mode: feed EQ  mode: feed EQ
DEx <sup>(1)</sup>	OSx <sup>(1)</sup> = NC	OSx <sup>(1)</sup> = 0	OSx <sup>(1)</sup> = 1			
NC (default)	0 dB	0 dB	0 dB			
1	-0.6 dB	-2.2 dB	-4.4 dB			
1	-6.0 dB	-6.2 dB	-6.2 dB			
1	-6.0 dB	-6.2 dB	-6.2 dB			
CONTROL PINS SETTINGS						
EN_RXD			DEVICE FUNCTION			
Normal Operation			Sleep Mode			
1 (default)			0			
(1) Where x = Channel 1 or Channel 2						
1	x	VIL	0	AESQ(1) = 0eH at 7.0Hz AQ(1,Q) IP programmable	same as Lane 0 to 2	DP mode: EQ fully programmable by AESQ(1); TMDs: default AQ(1); EQ setting at 8.0Hz at 7.0Hz
		VHI	x		3dB at 1.35GHz	TMDs: mode: EQ disabled



# USB HUB



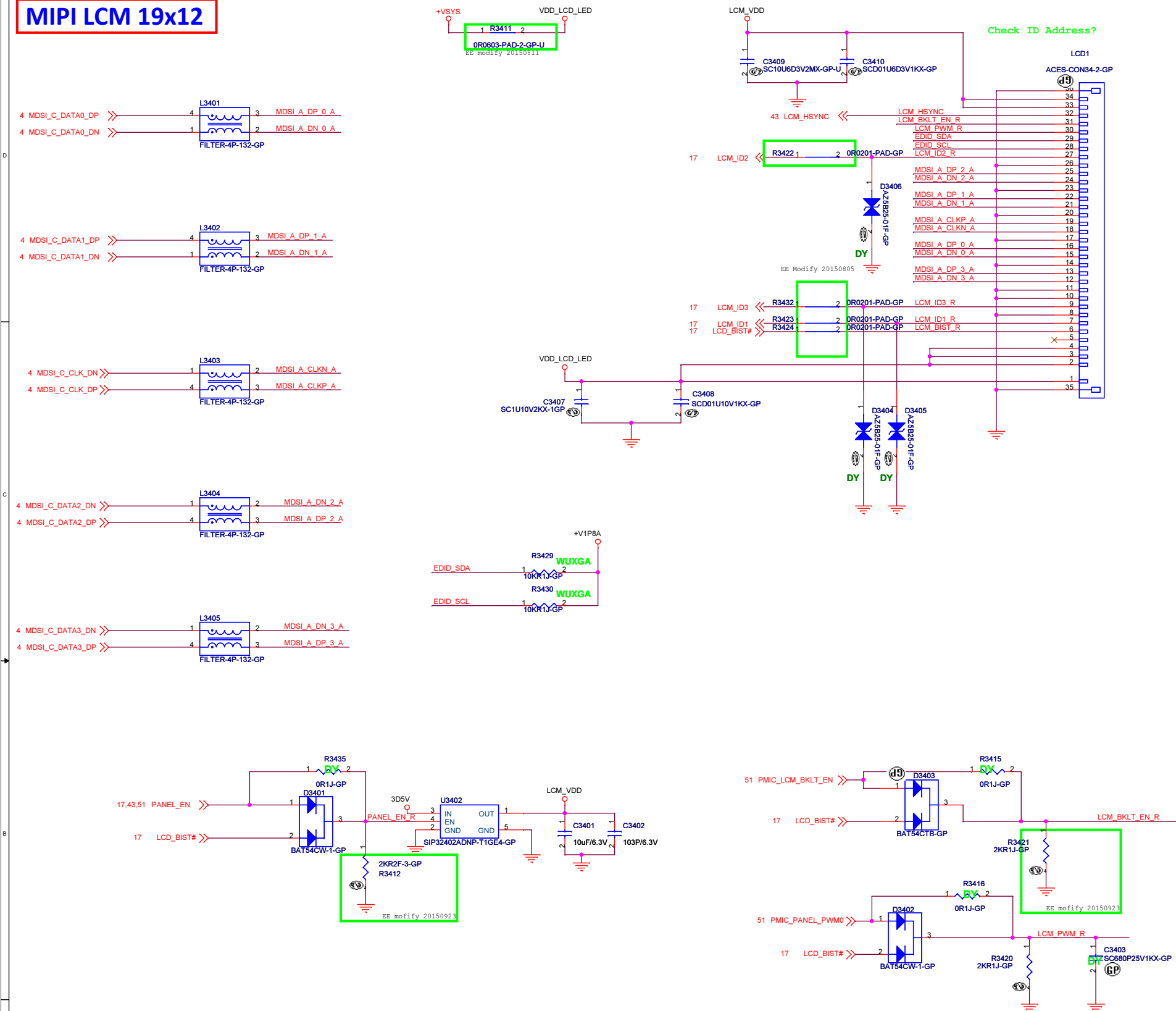
## USB HUB



```
OVCURn#
Floating      : Non-removable
Pull high    : Removable
```

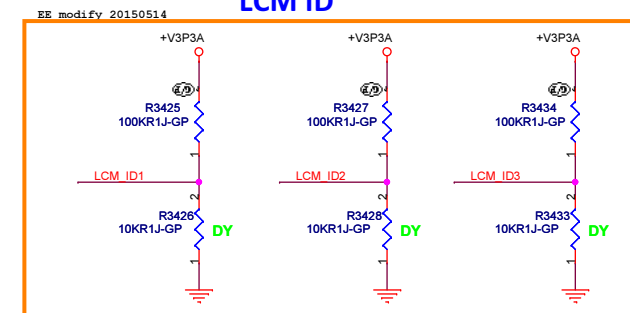


## MIPI LCM 19x12



No.	Pin Name	Pin Name Description
1	VDD	DC-DC circuit supply voltage (3V~3.6V)
2	VDD	DC-DC circuit supply voltage (3V~3.6V)
3	H <sub>sync</sub>	H <sub>sync</sub>
4	LED_EN	LED driver Enable Input (VIH=1.8V)
5	LED_PWM	Backlight LED driver PWM Input (VIH=1.8V)
6	EDIO_SDA	EDIO Data Input (VIH=1.8V)
7	EDIO_SCL	EDIO Clock Input (VIH=1.8V)
8	ID	NC
9	GND	Ground
10	DSI_D2P/Rx-IN2P	MIPI data pair 2 positive signal
11	DSI_D2N/Rx-IN2N	MIPI data pair 2 negative signal
12	GND	Ground
13	DSI_D1P/Rx-IN1P	MIPI data pair 1 positive signal
14	DSI_D1N/Rx-IN1N	MIPI data pair 1 negative signal
15	GND	Ground
16	DSI_CLKP/Rx-CLKP	MIPI Clock positive signal
17	DSI_CLKN/Rx-CLKN	MIPI Clock negative signal
18	GND	Ground
19	DSI_D0P/Rx-IN0P	MIPI data pair 0 positive signal
20	DSI_D0N/Rx-IN0N	MIPI data pair 0 negative signal
21	GND	Ground
22	DSI_D3P/Rx-IN3P	MIPI data pair 3 positive signal
23	DSI_D3N/Rx-IN3N	MIPI data pair 3 negative signal
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	ID	Ground
29	BIST	Aging Mode Power Supply
30	NC	Not Connection
31	LED+	LED Power Supply (3V ~ 5V)
32	LED+	LED Power Supply (3V ~ 5V)
33	LED+	LED Power Supply (3V ~ 5V)
34	LED+	LED Power Supply (3V ~ 5V)

## LCM ID



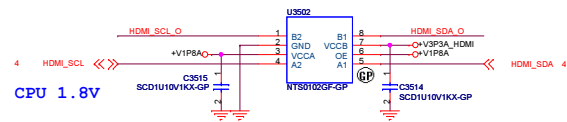
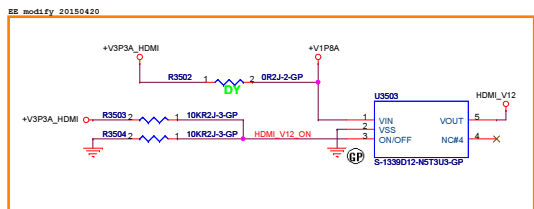
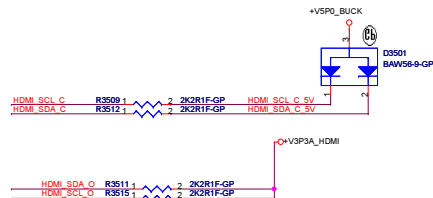
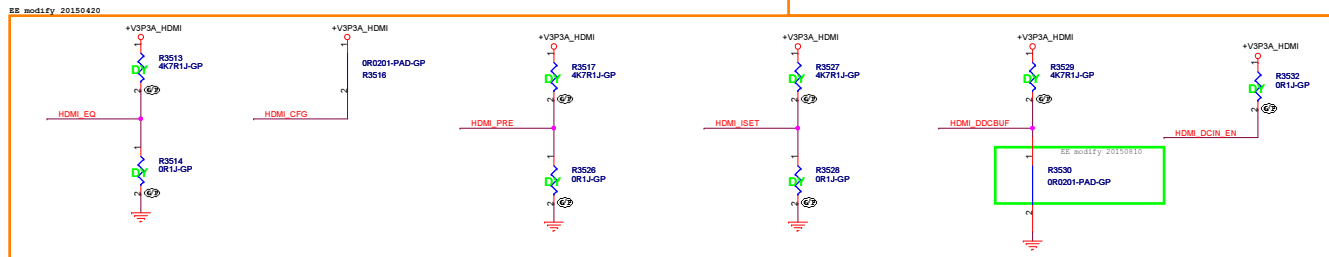
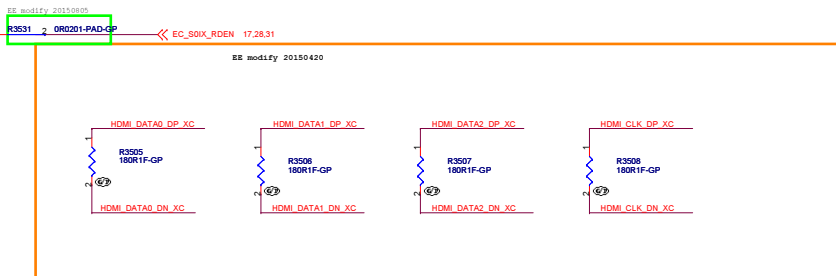
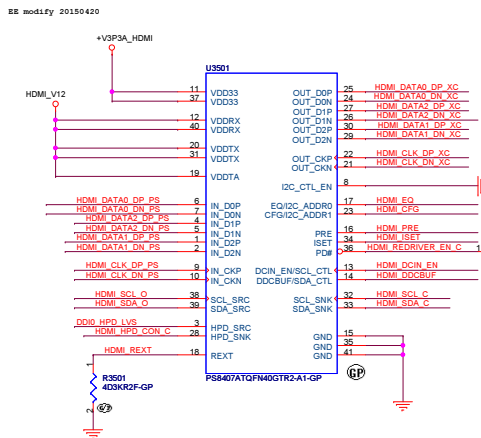
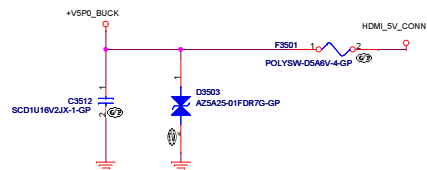
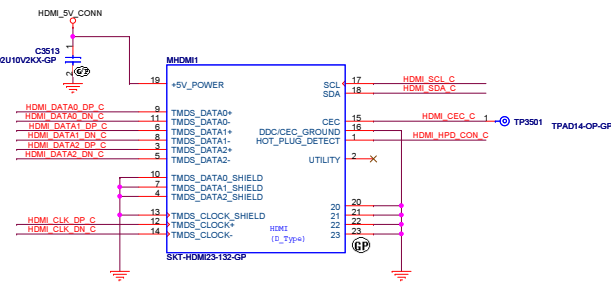
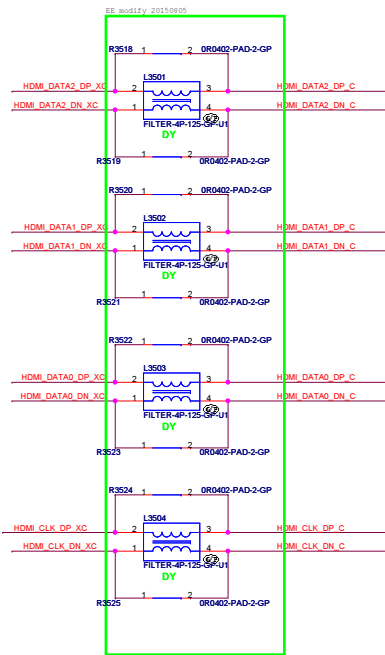
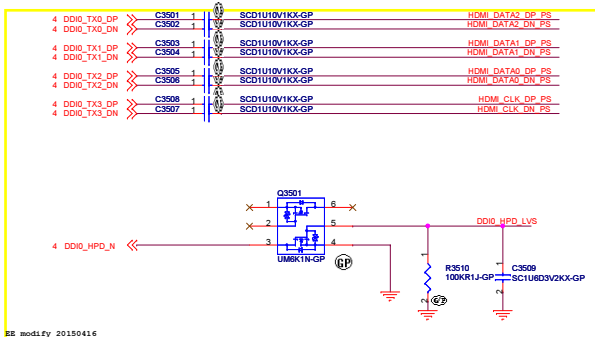
	LCM_ID1	LCM_ID2	LCM_ID
AUO	H	H	L
BOE	H	L	L
NO Panel	H	H	H

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Each port I/O has an internal  
10 k  $\Omega$  pull-up resistor to VCC(A)/VCC(B)



**Device :uHDMI**




Pin	Pin 定義
1	Hot Plug Detect
2	Utility
3	TMDS Data2+
4	TMDS Data2- Shield
5	TMDS Data2-
6	TMDS Data1+
7	TMDS Data1- Shield
8	TMDS Data1-
9	TMDS Data0+
10	TMDS Data0- Shield
11	TMDS Data0-
12	TMDS Clock+
13	TMDS Clock- Shield
14	TMDS Clock-
15	CEC
16	DDC/CEC Ground
17	SCL
18	SDA
19	+5V Power

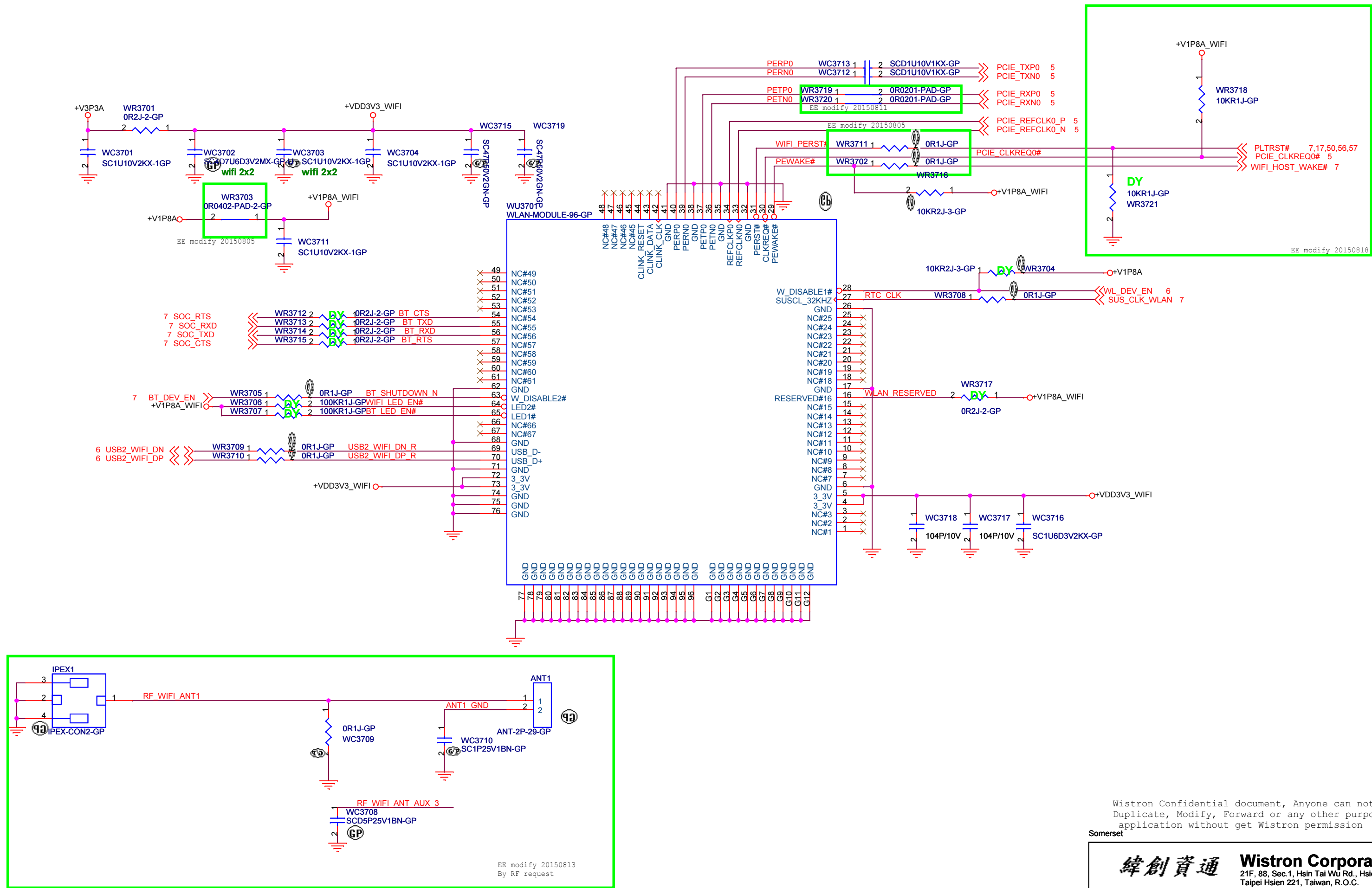
5	4	3	2	1
D				D
C				C
B				B
A				A

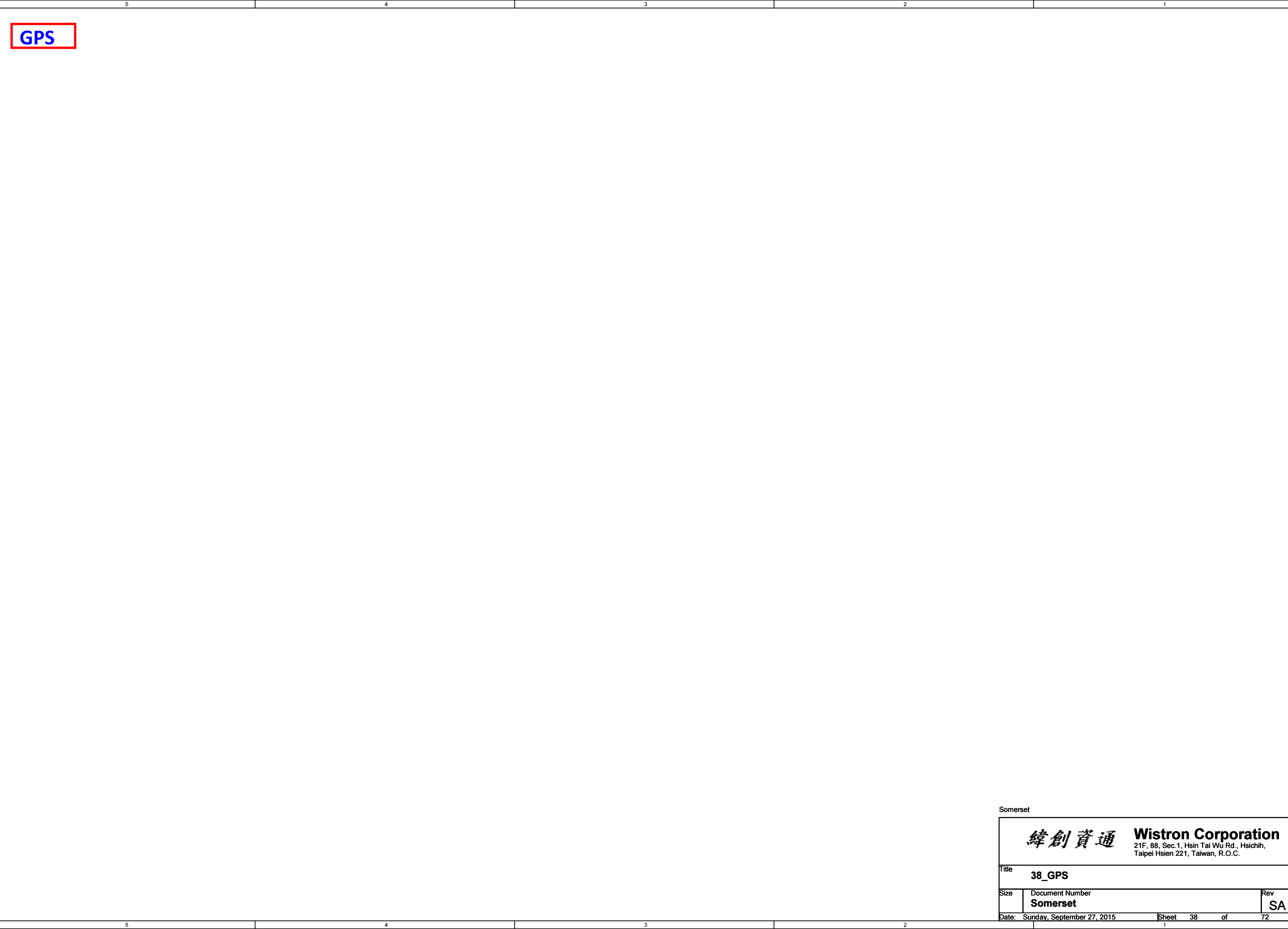
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Title <b>36_Display Port</b>			
Size	Document Number <b>Somerset</b>		Rev <b>SA</b>
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# WIFI/BT 2X2SFP



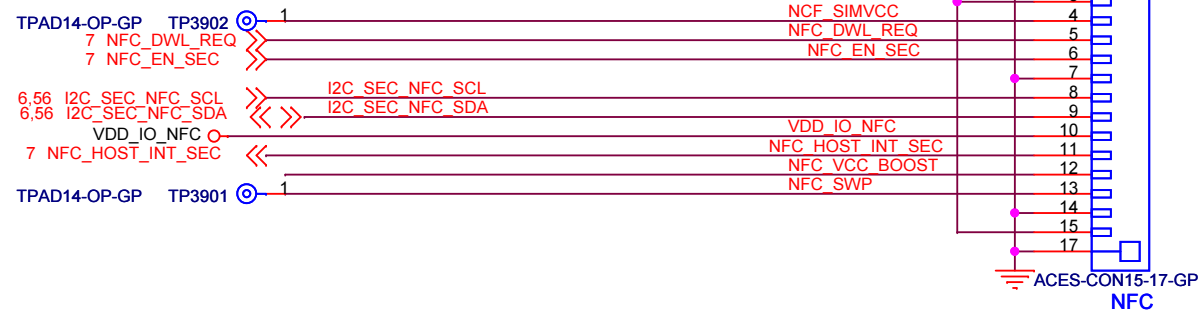
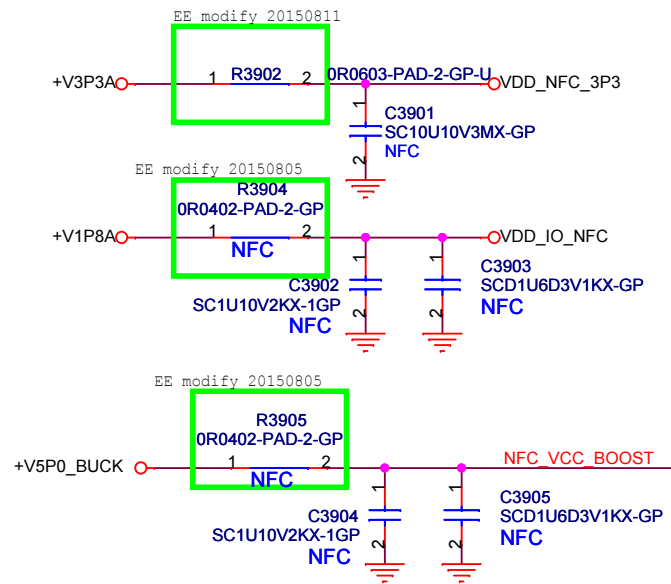


GPS

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Title <div>38_GPS</div>	
Size <div></div>	Rev <div>SA</div>
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NFC



NFC used Module Type

Pin number	Name
1	MOD_VDD
2	MOD_GND
3	SWP
4	VCC_BOOST
5	IRQ
6	PMUVCC
7	I <sup>2</sup> C_SDA
8	I <sup>2</sup> C_SCL
9	MOD_GND
10	Reset/Wakeup
11	DWL_REQ
12	SIMVCC
13	MOD_VDD
14	VDD_IO
15	MOD_GND

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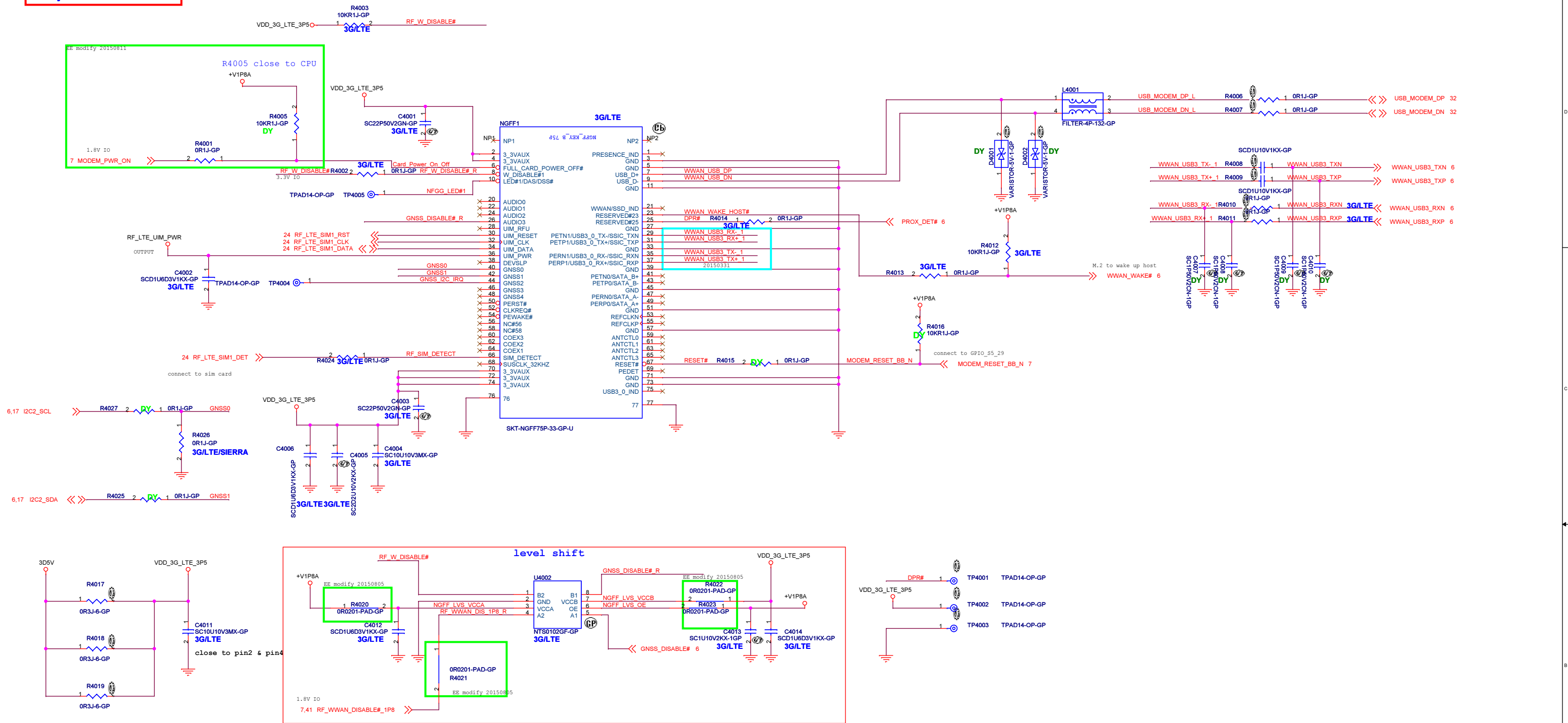
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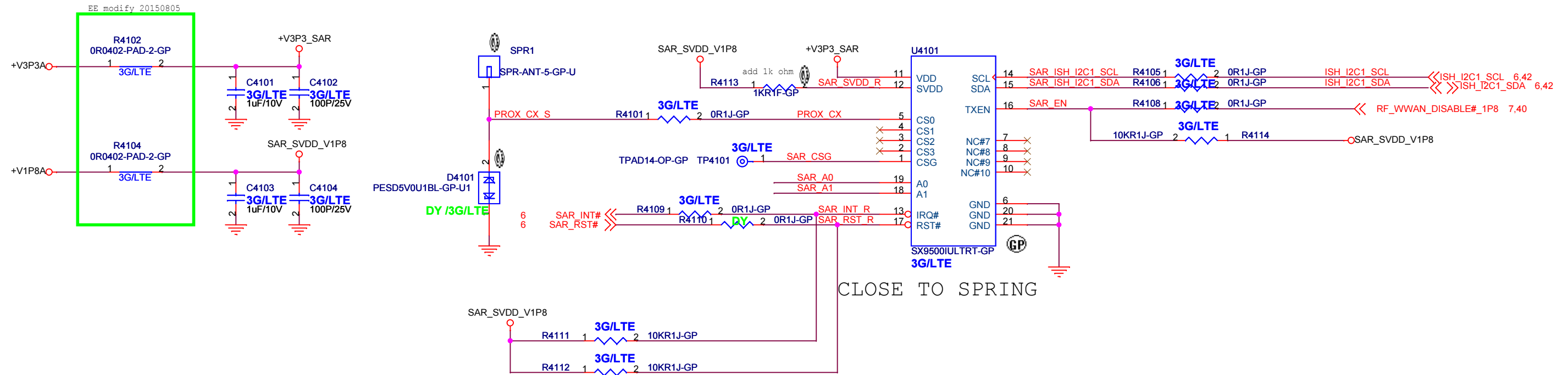
Title 39_NFC		
Size	Document Number Somerset	Rev SA
Date: Sunday, September 27, 2015 Sheet 39 of 72		



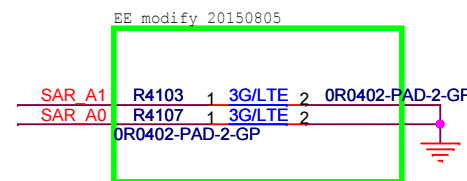
# 3G/LTE module



## SAR sensor for 3G/LTE



A1	A0	Address
0	0	0x28
0	1	0x29
1	0	0x2A
1	1	0x2B



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緯創資通

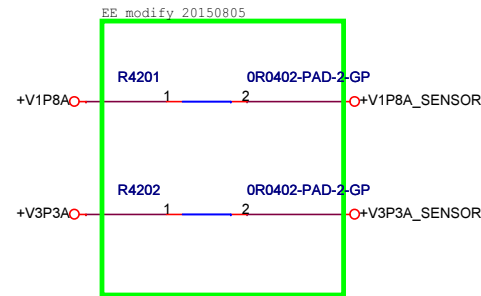
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>41_SAR Sensor</b>
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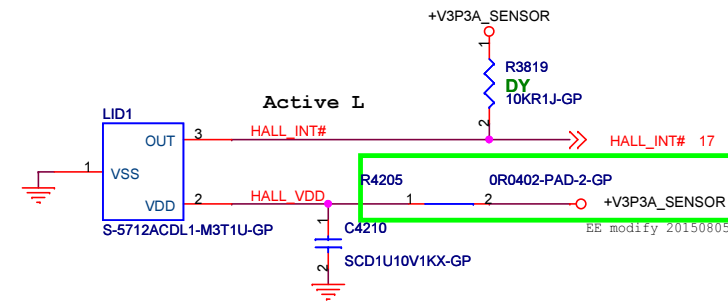
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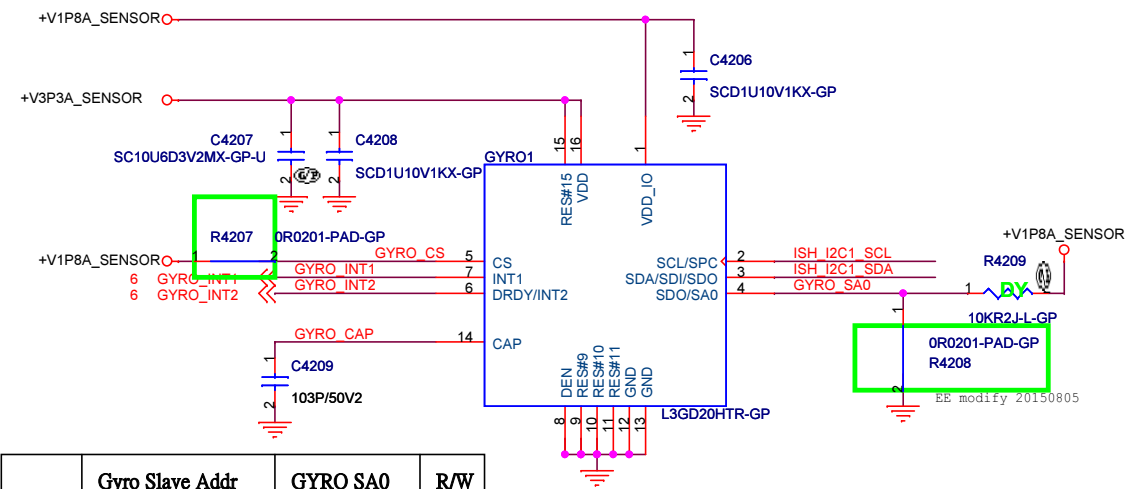
Date: Sunday, September 27, 2015 Sheet 41 of 72



## HALL Sensor



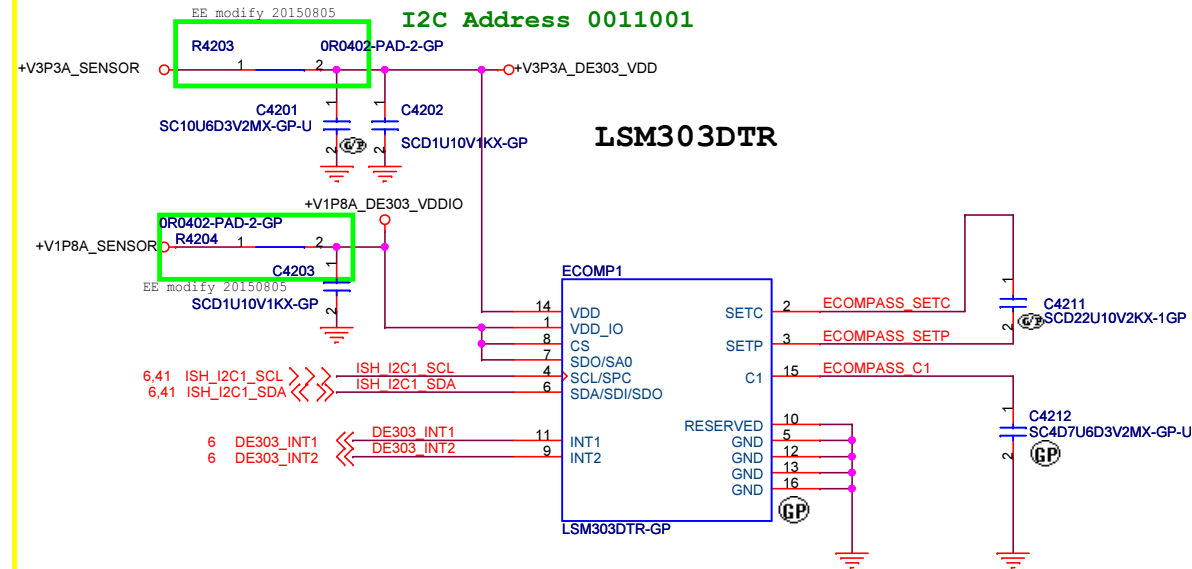
## Gyro Sensor I2C Address 1101010



	Gyro Slave Addr	GYRO SA0	R/W
D4	Write	110101	0
D5	Read	110101	0

## G Sensor + E-Compass

I2C Address 0011001



	G-Sensor Slave Addr	R/W
3A	Write	0011,101
3B	Read	0011,101

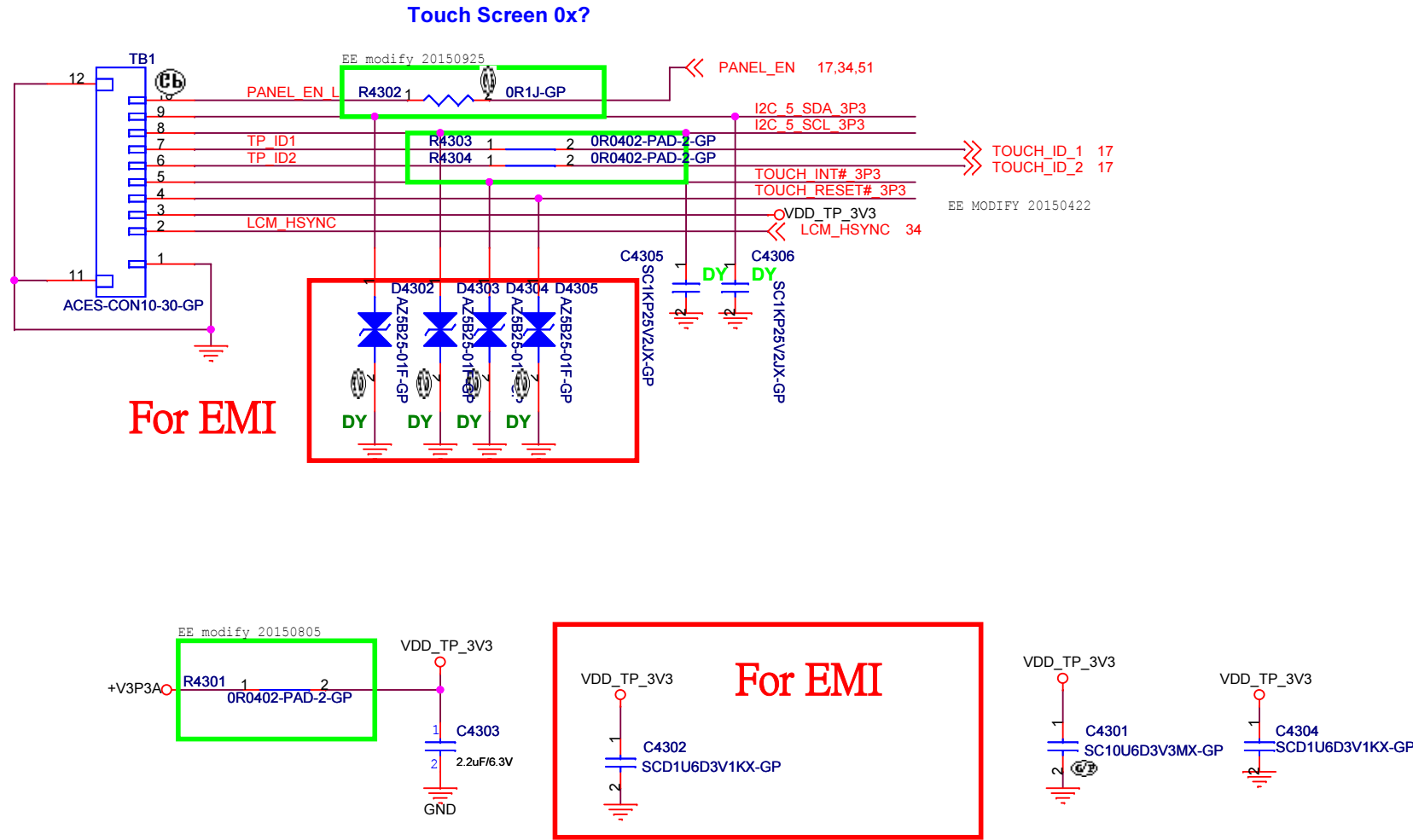
	e-Compass Slave Addr	R/W
3C	Write	0011,110
3D	Read	0011,110

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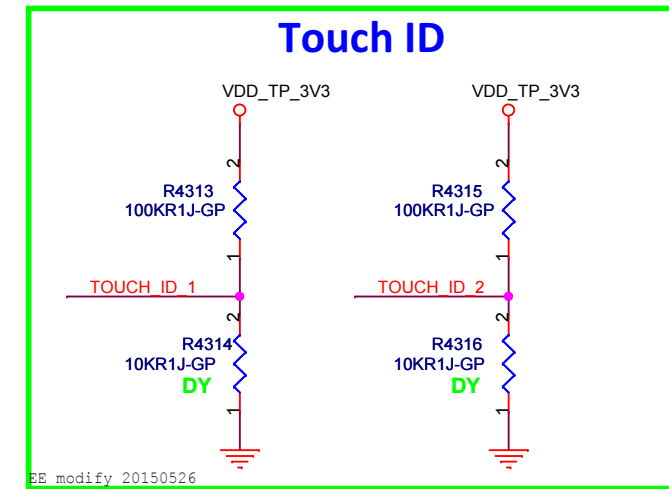
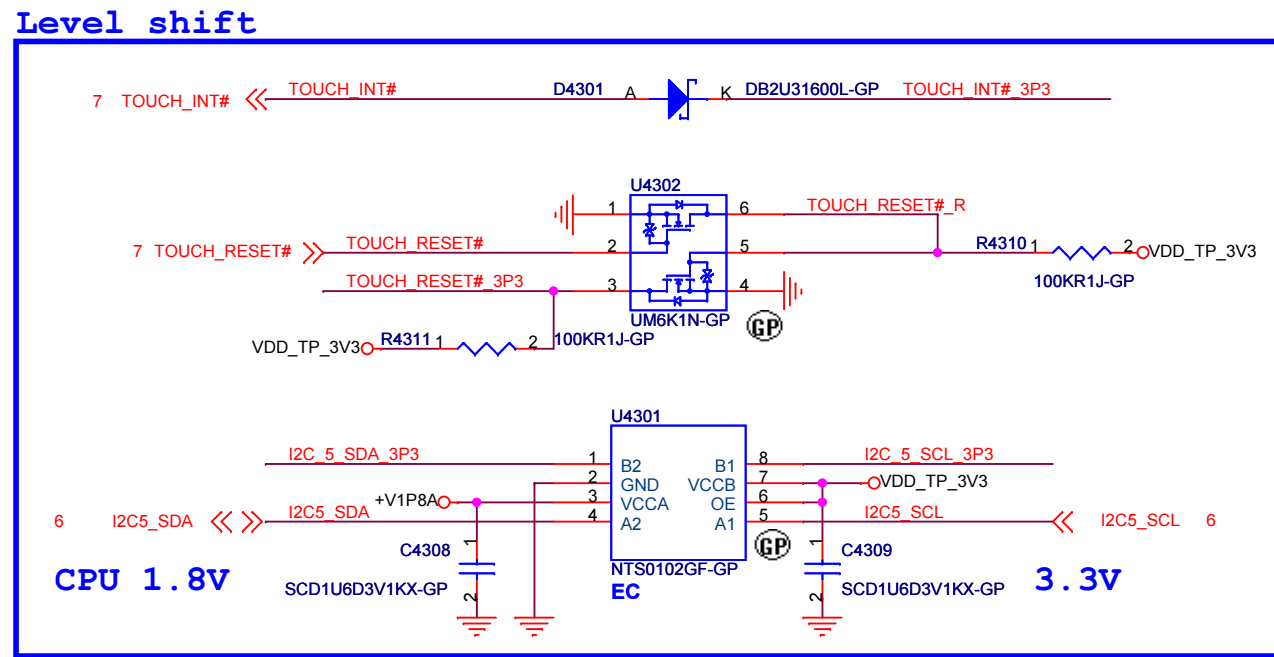
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Title 42_Sensor	
Size	Document Number Somerset
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# Touch Panel

CN1 PIN #	Host 接続時	Description
1	NC	Keep Open
2	SDA	IIC Data Open drain; pull-up resistor at Host is needed
3	SCL	IIC Clock Open drain; pull-up resistor at Host is needed
4	ID01	Touch Sensor Identification Pin 01
5	ID02	Touch Sensor Identification Pin 02
6	IRQ	IIC Data Ready Output "LOW" when data ready to send Open drain; pull-up resistor at Host is needed
7	RESET	RESET Stop operation when pull "LOW" Build-in pull-up resistor 100kohm
8	VDD +3.3V	3.3volt power input
9	HSYNC	LCD Hsync input
10	GND	Ground



	ID1	ID2
	ID01 (Pin 4)	ID02 (Pin 5)
HH	NC	NC
TPK	NC	GND
O-Film	GND	NC
Option2	GND	GND



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43_Touch Panel	
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Sheet 43 of 72	SA

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D

C

C

B

B

A

A

5

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4

3

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55

**Somerset**

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>44_LED BOOST</b>
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Size B	Document Number <b>Somerset</b>
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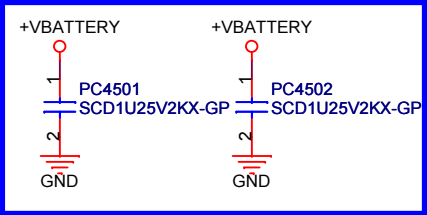
Rev	0
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Date: Sunday, September 27, 2015

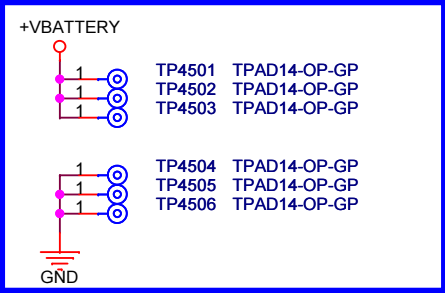
Sheet 44 of 72

BATTERY CONN

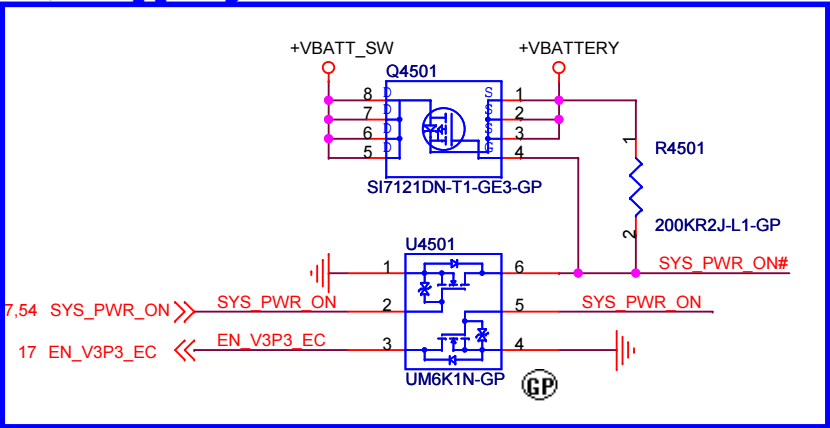
For EMI



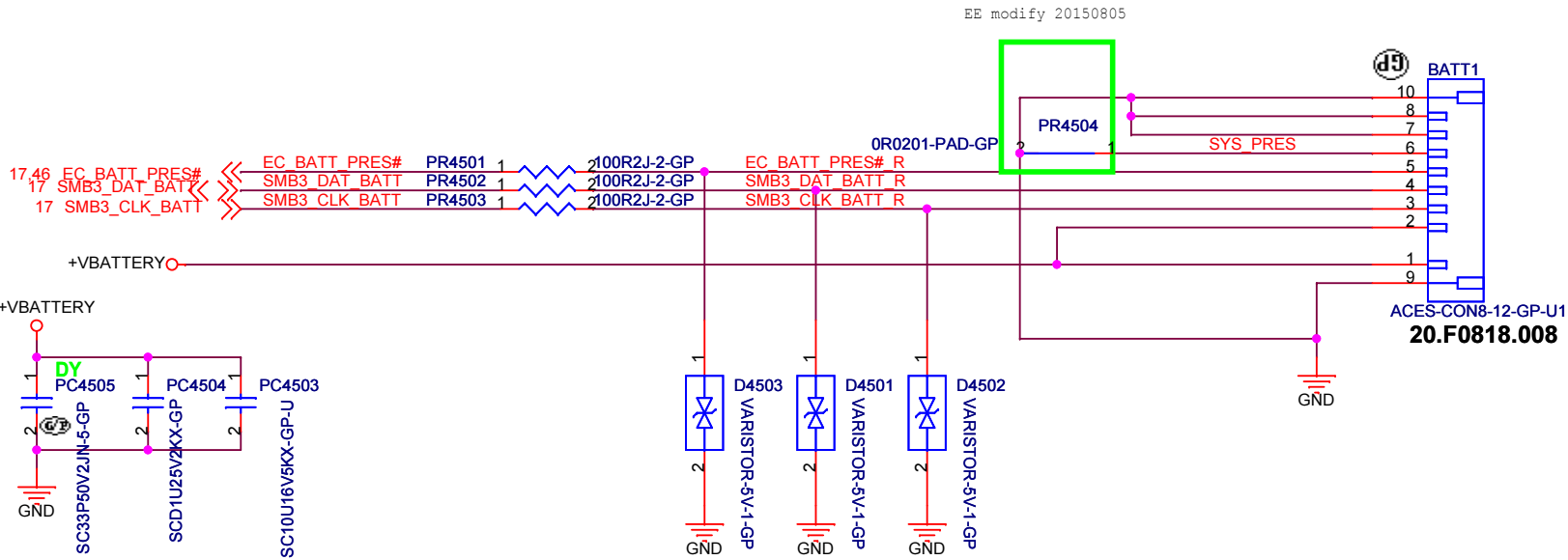
For Test



S5/Shipping mode



Battery Connector



Pin #	Signal	Description/Function	Color
1	BATT+	Power, Batt +, Positive terminal of battery stack	Red
2	BATT -	Power, Batt -, Negative terminal of battery stack	Red
3	CLK_SMB	System Management Bus Clock	Blue
4	DAT_SMB	System Management Bus Data	White
5	BATT_PRS*	Battery Present (This is tied to ground on the Battery Pack)	Yellow
6	SYS_PRES*	System Present (This is tied to ground on the system side)	Green
7	GND	Power, Batt -, Negative terminal of battery stack	Black
8	GND	Power, Batt -, Negative terminal of battery stack	Black

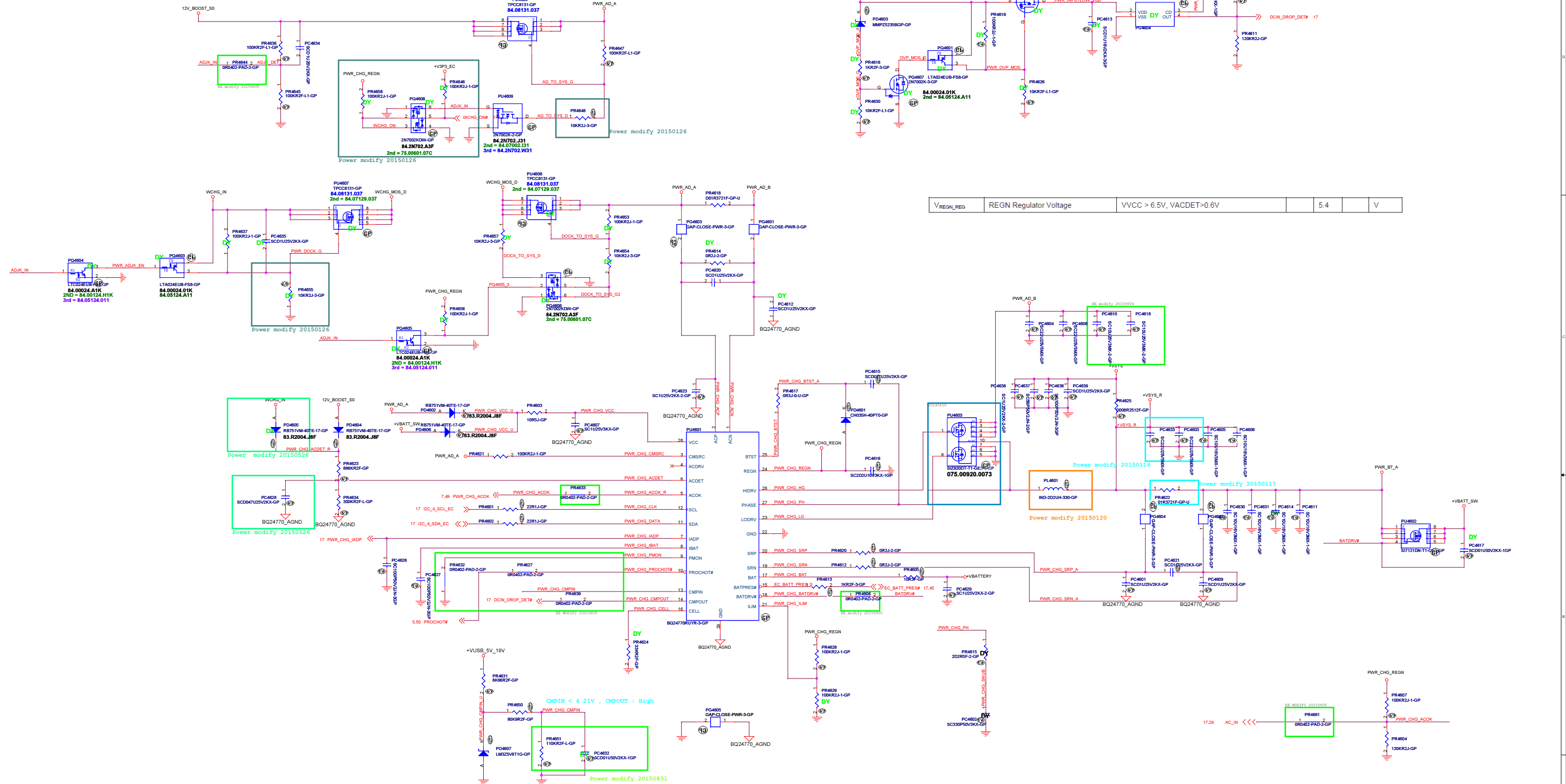
Somerset	Connector type: WTB, 8Pin
	Connector: Aces 50280-010H0H0-001
	Per. Pin Rating: 1.8A/Per pin

WIRELESS CHARGE

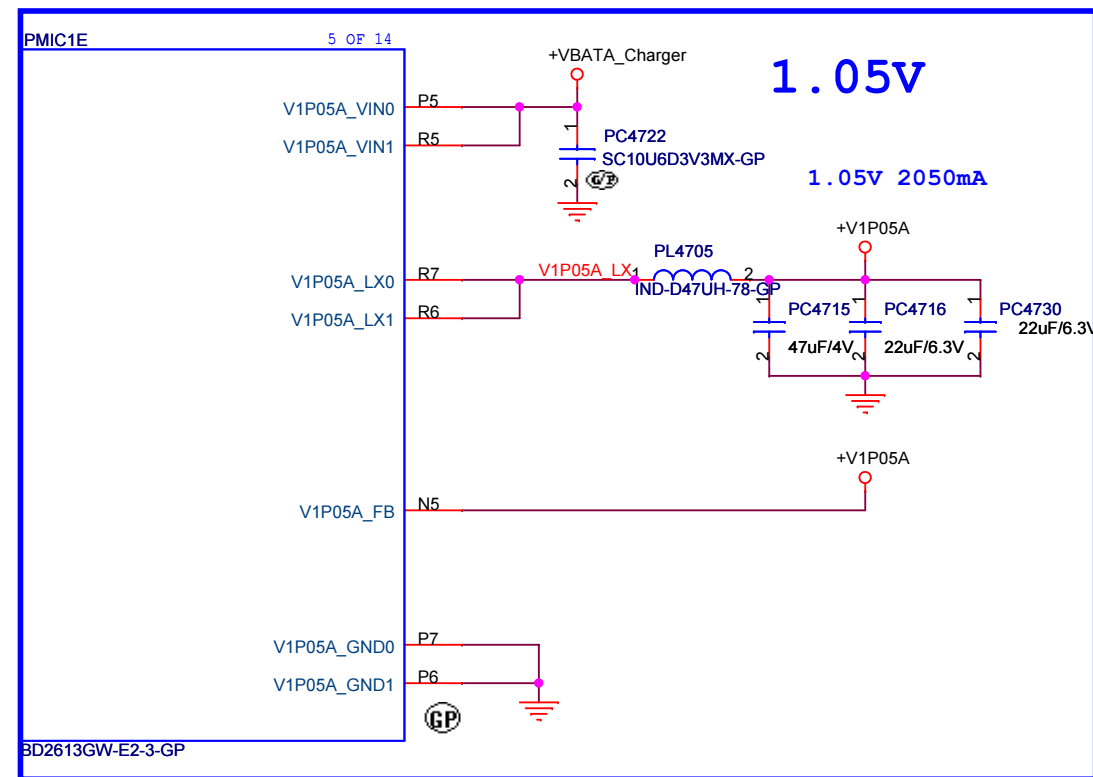
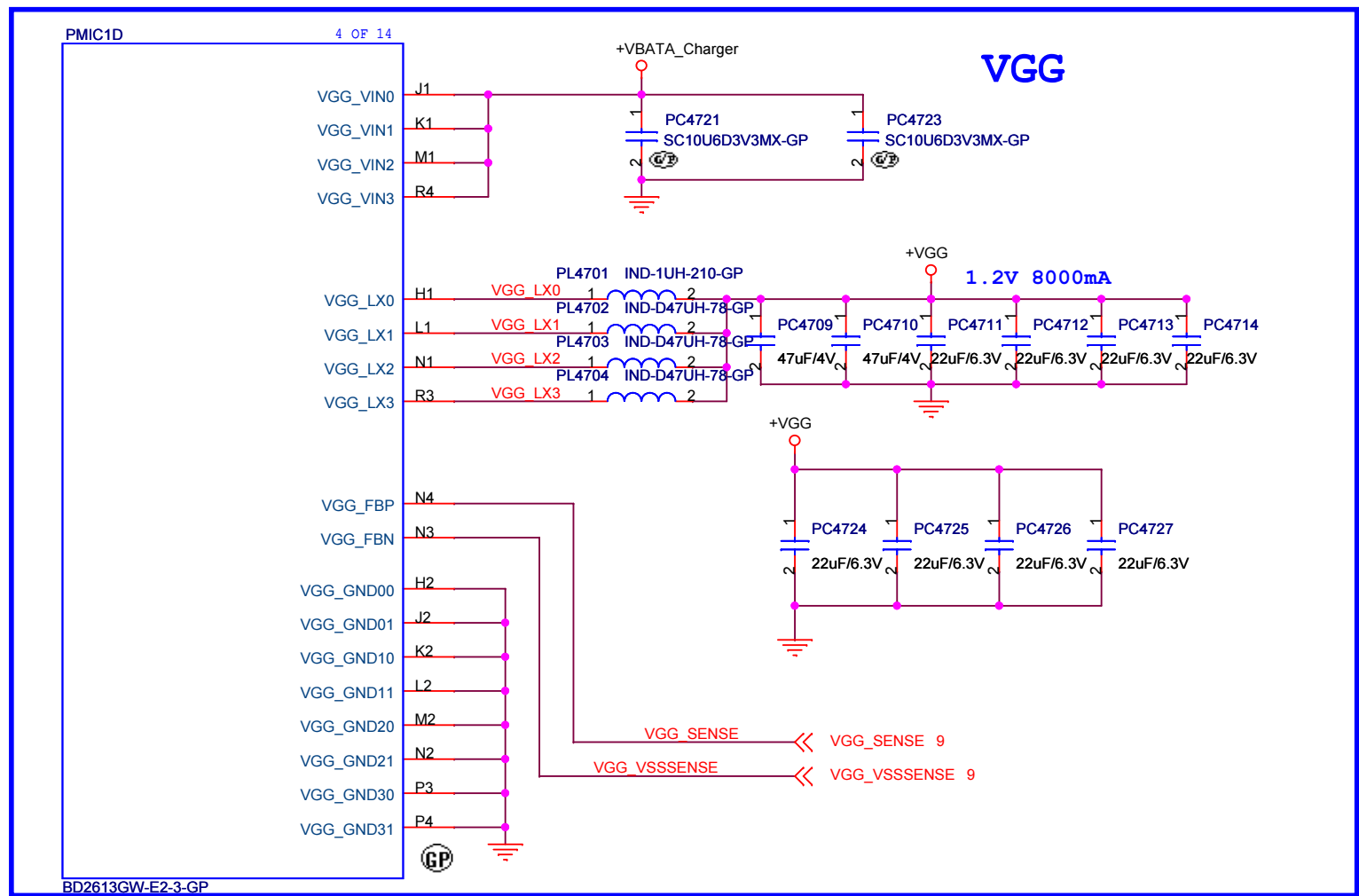
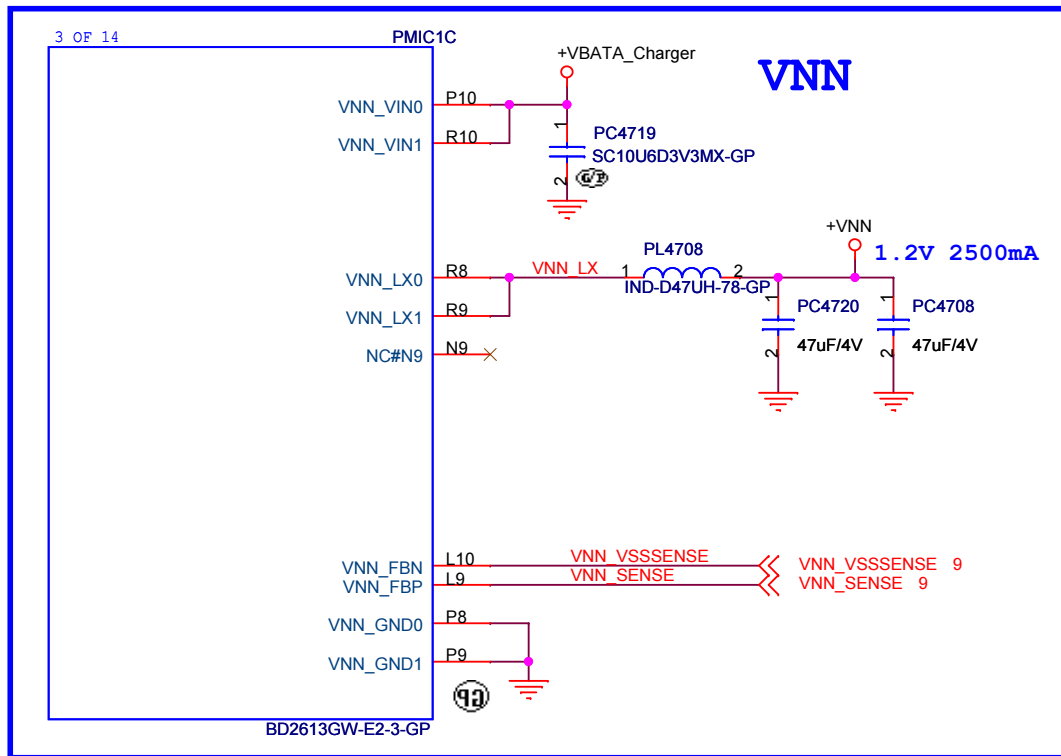
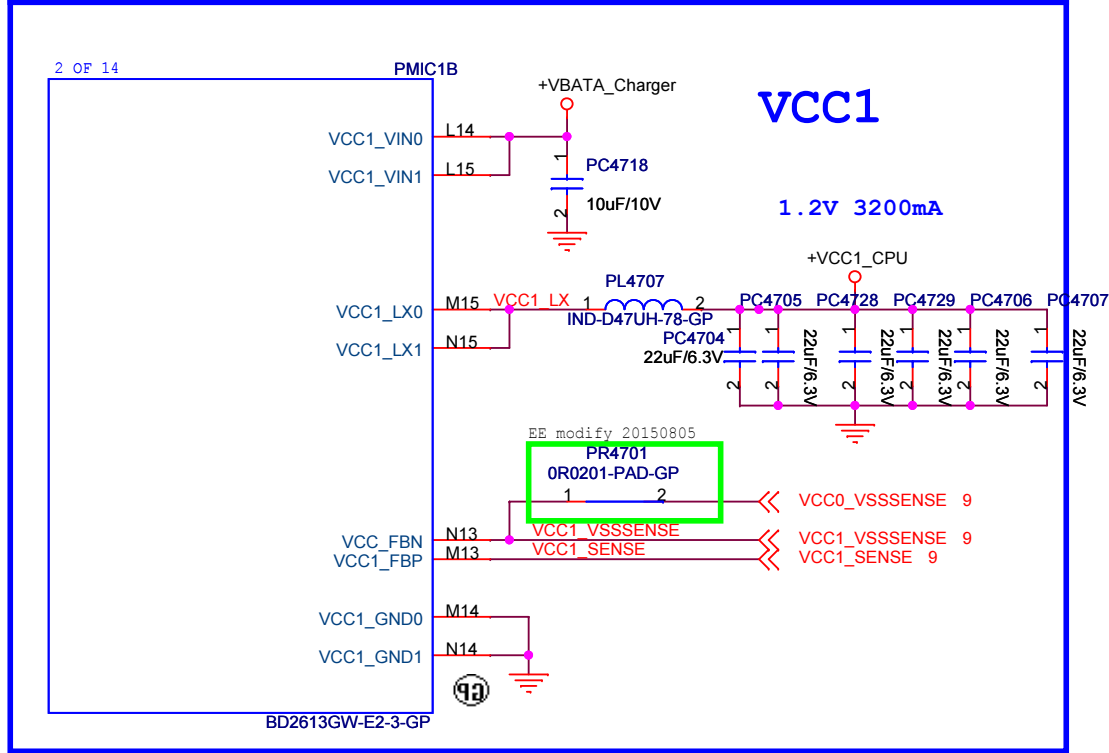
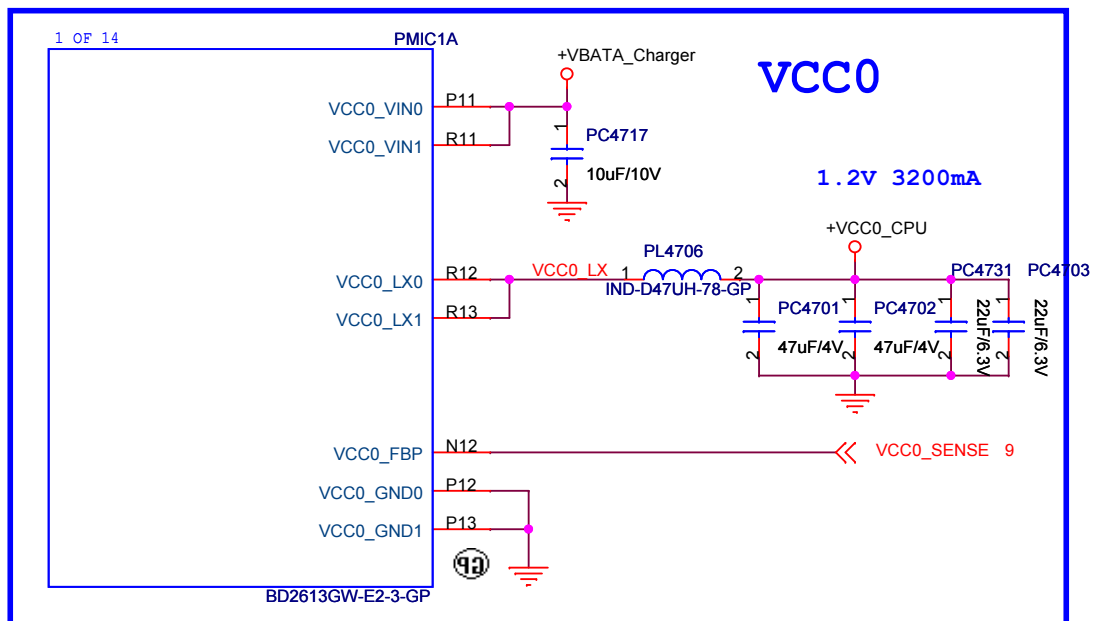
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# Charger



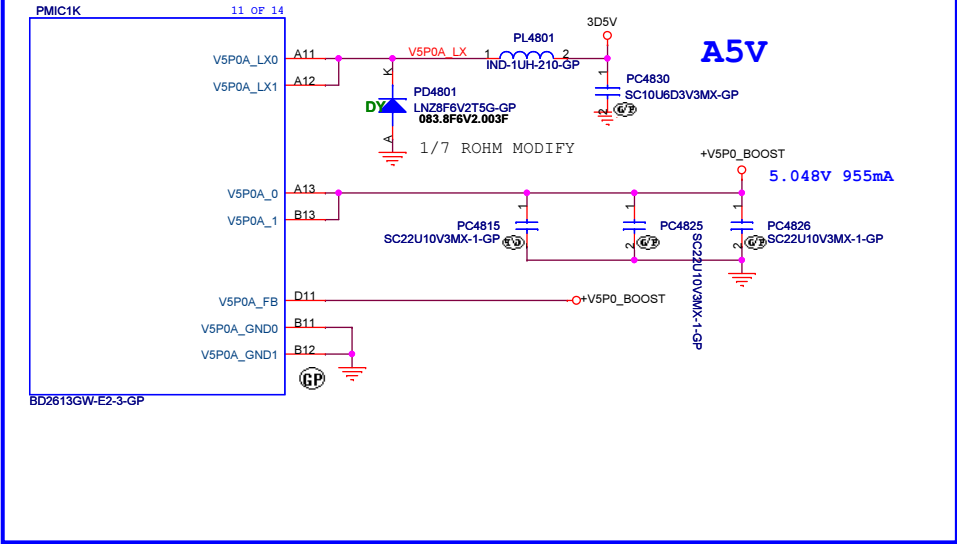
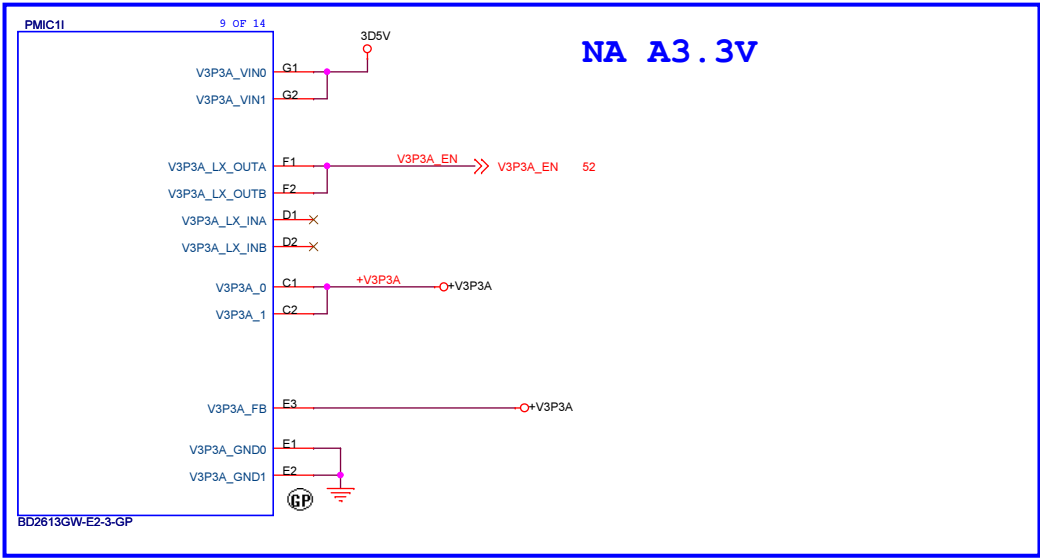
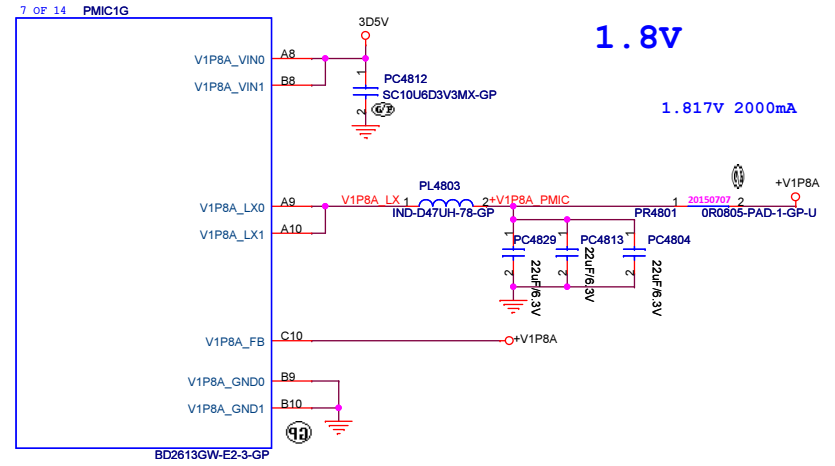
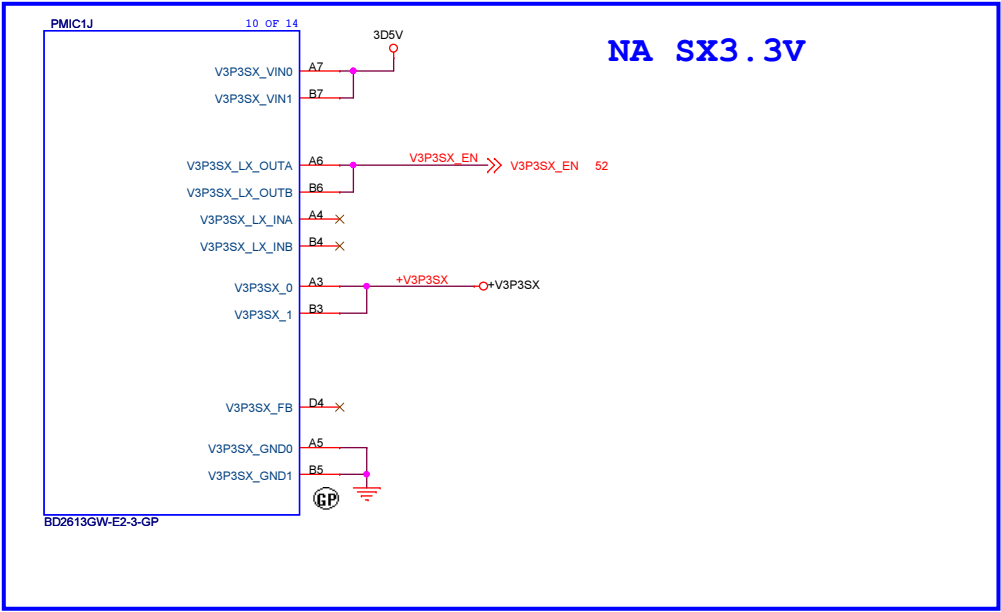
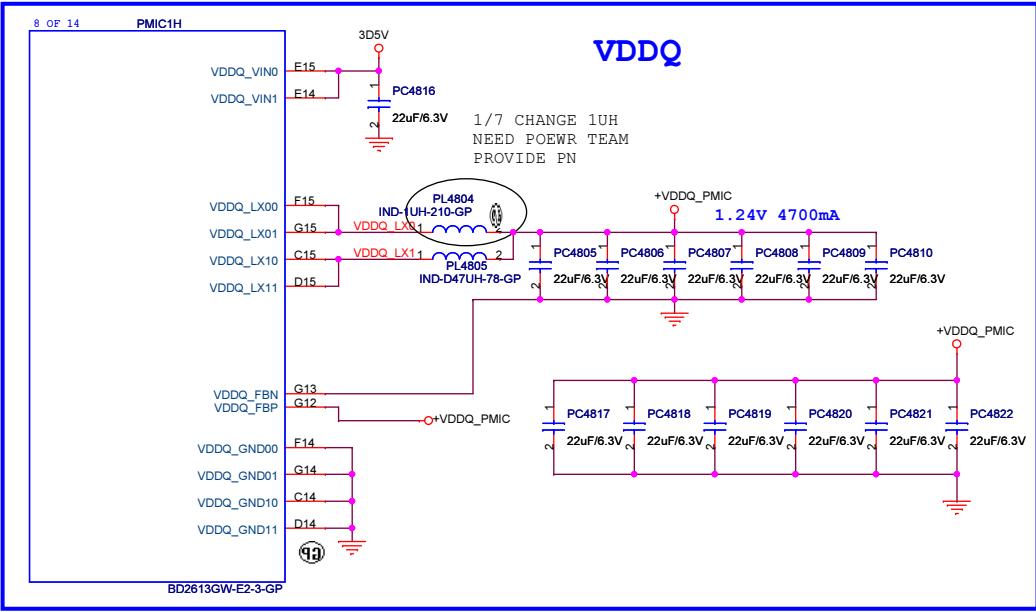
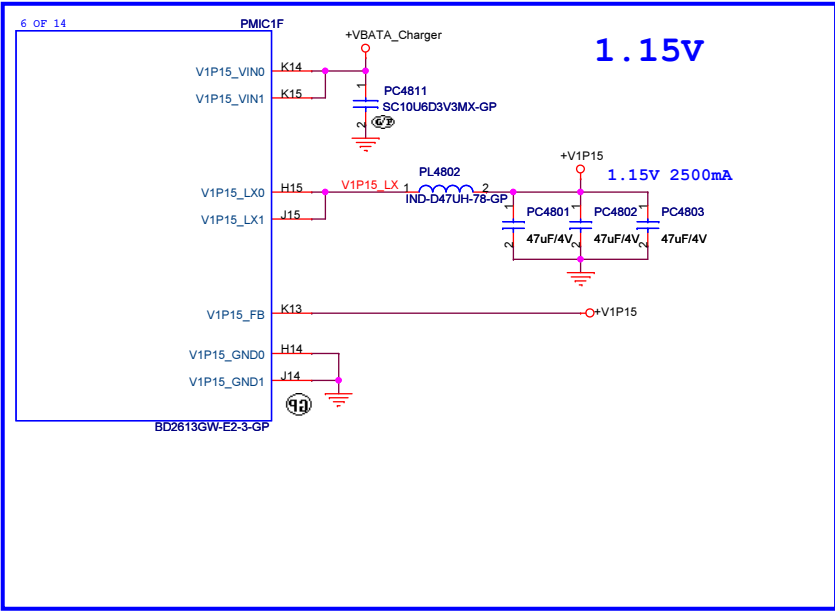
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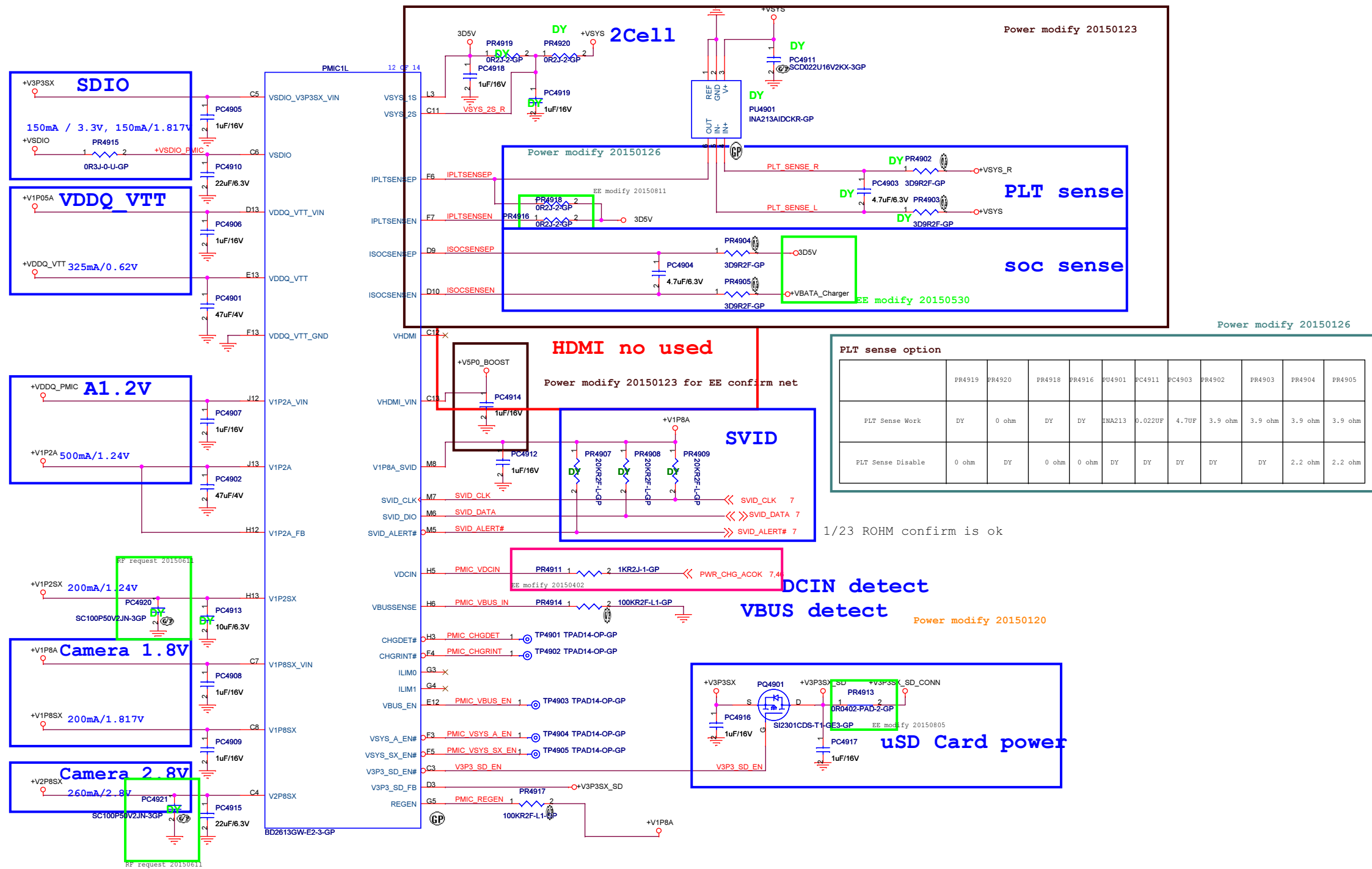
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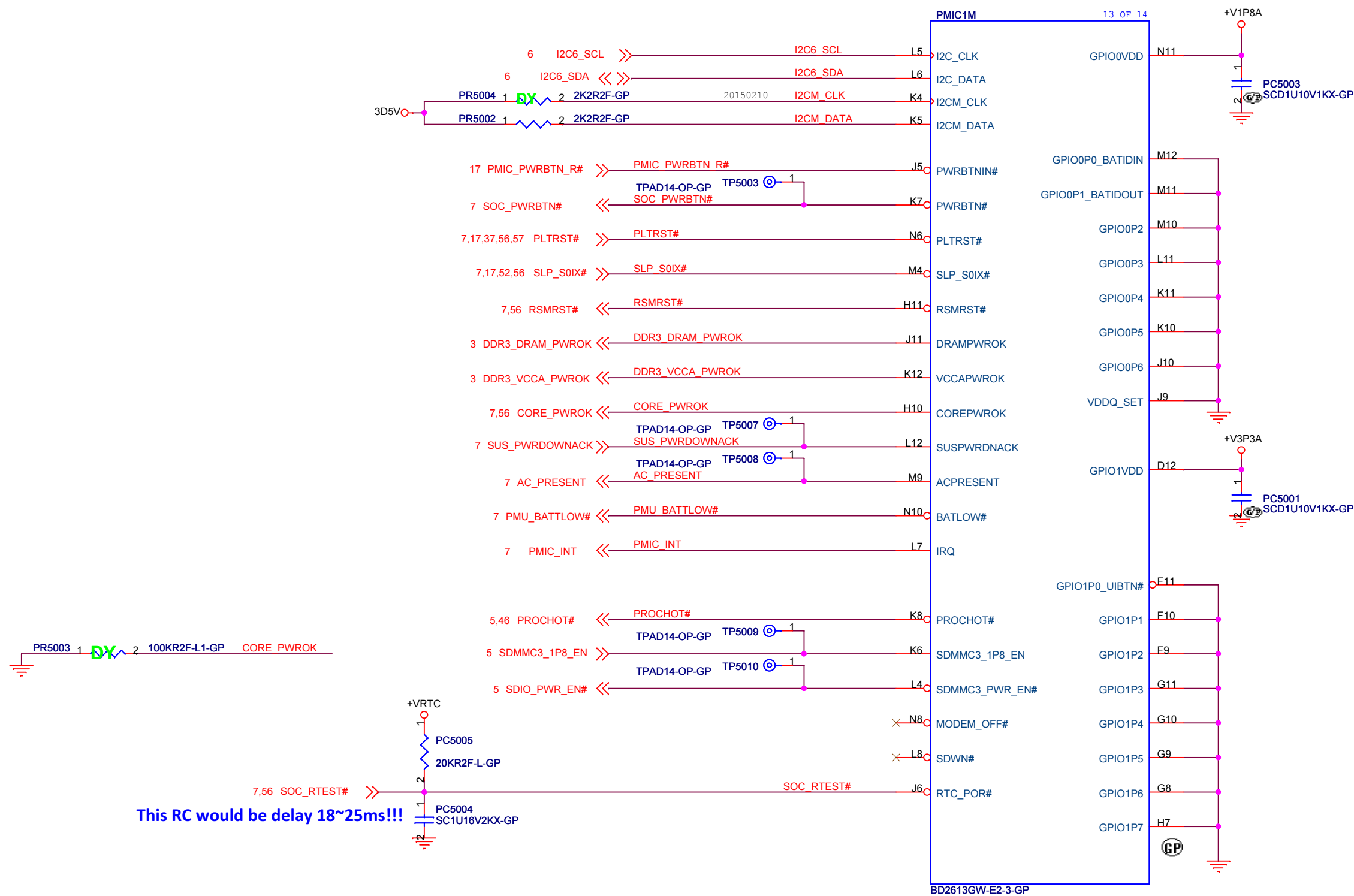
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<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p> <p>47 PMIC(1/5) (BD2613)</p>	
<p>Size</p> <p>Document Number</p> <p>Somerset</p>	<p>Rev</p> <p>SA</p>
<p>Date: Sunday, September 27, 2015</p> <p>Sheet 47 of 72</p>	



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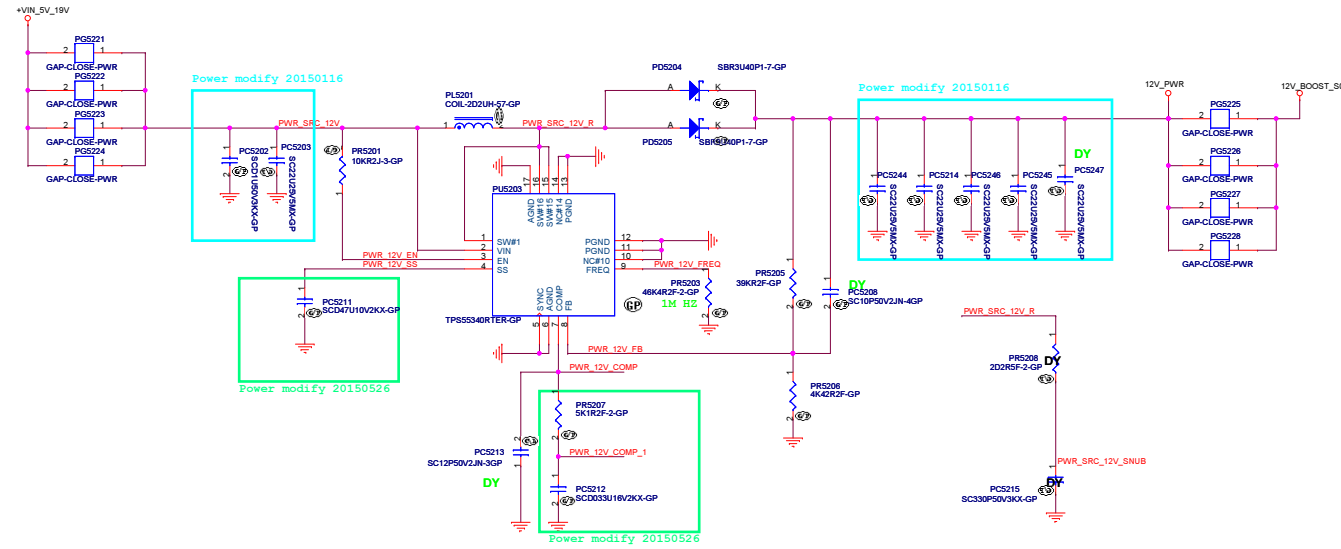


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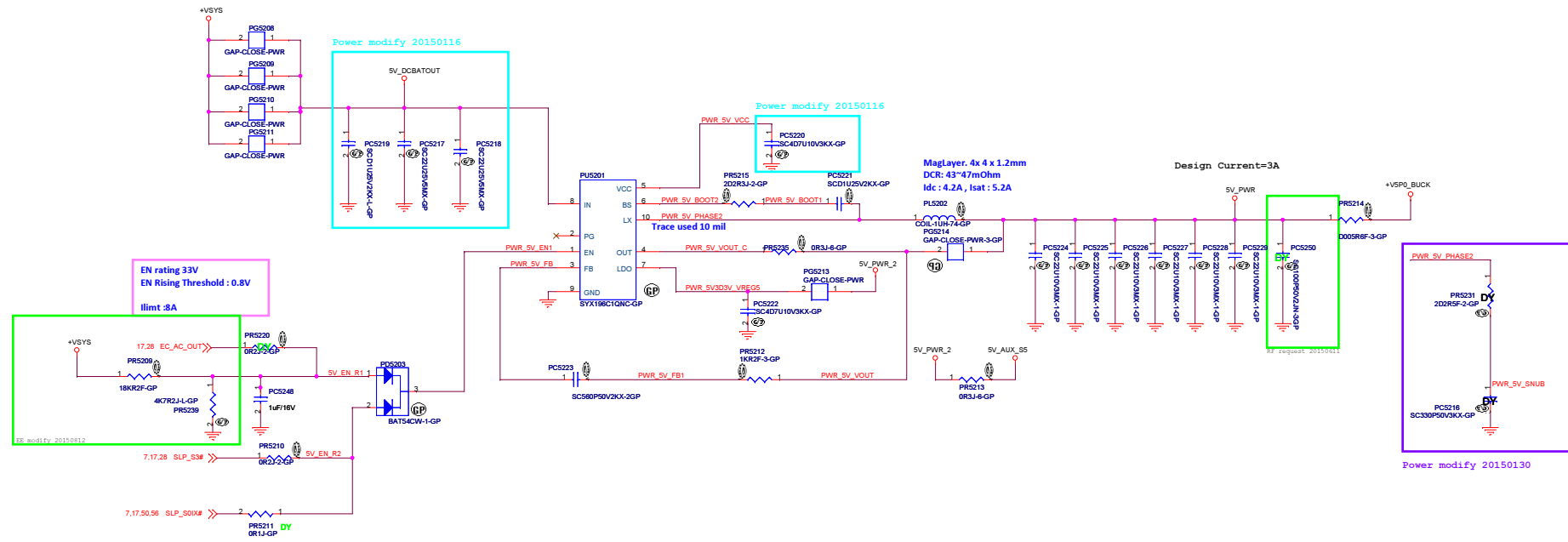
Somerset

Title		50 PMIC(4/5) (BD2613)	
Size	Document Number	Rev	
	Somerset	SA	
Date:	Sunday, September 27, 2015	Sheet	50 of 72

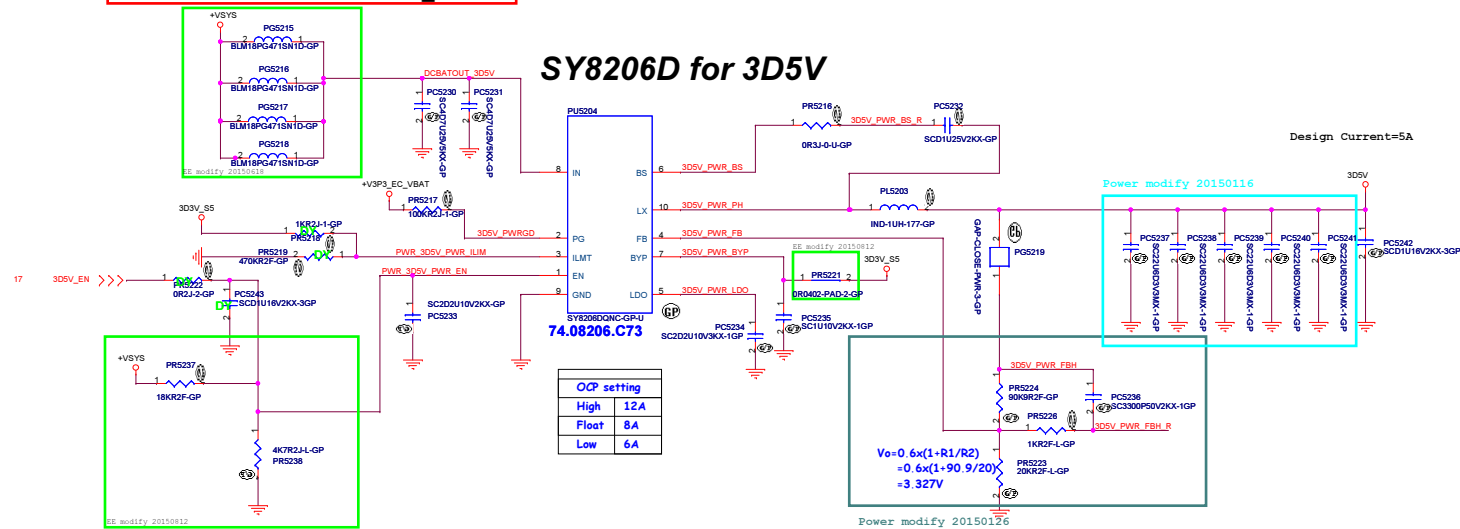




## 5V BUCK

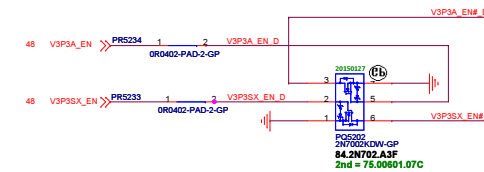


## SSID = PWR.Plane.Regulator\_3D5V

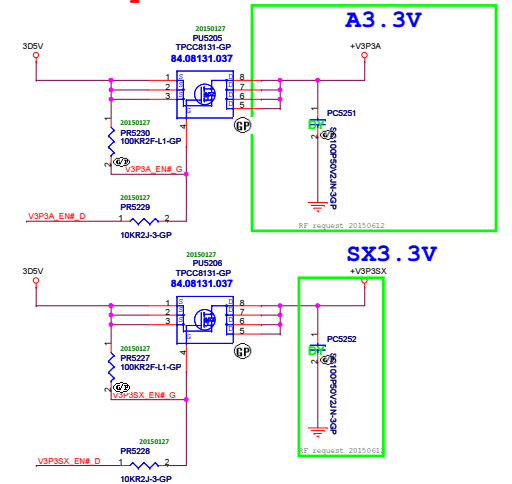


OCP setting	
High	12A
Float	8A
Low	6A

$$V_o = 0.6 \times (1 + R_1/R_2) = 0.6 \times (1 + 90.9/20) = 3.327V$$



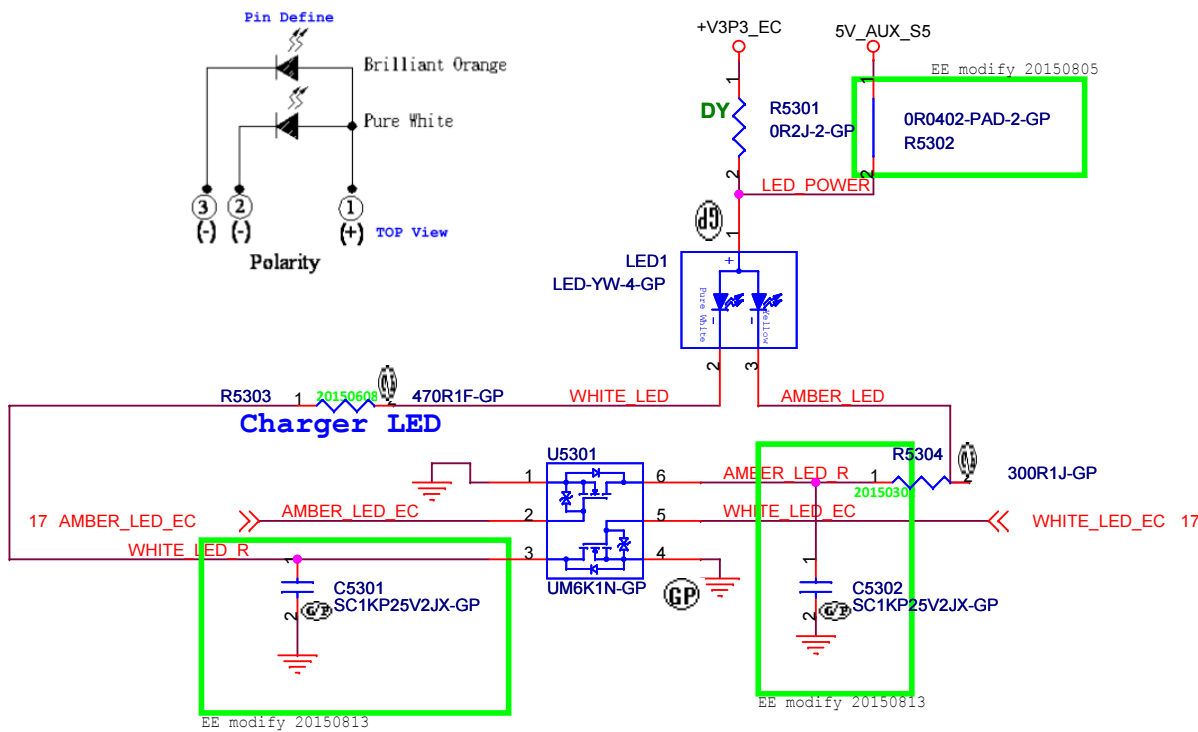
## EE Modify20150402



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POWER LED



WIRELESS LED

USB HSIC HUB

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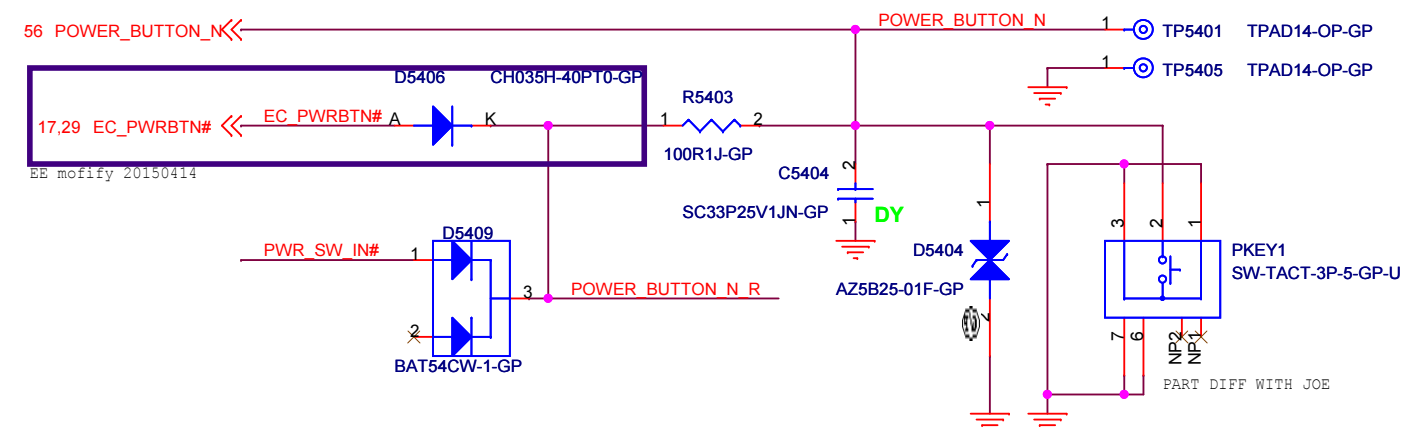
Title  
**53\_POWER LED/DOCK CONN**

Size  
Document Number  
**Somerset**

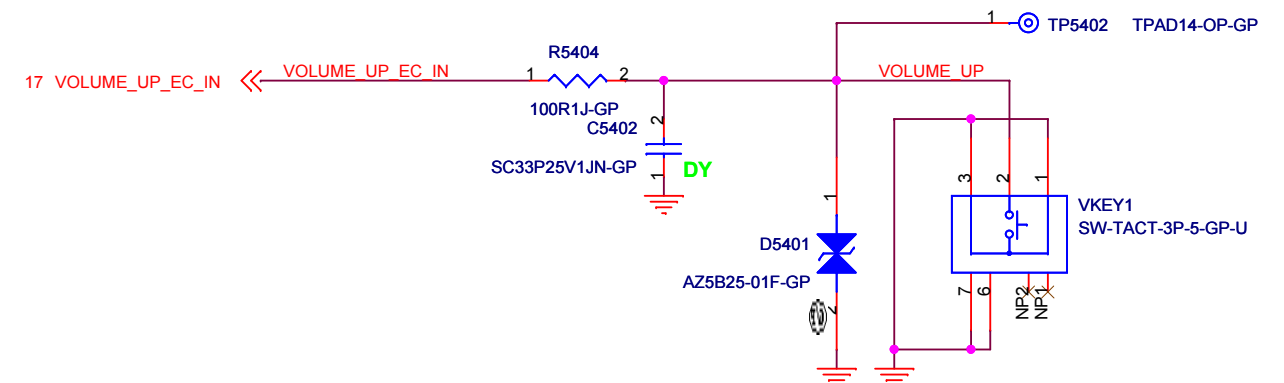
Rev  
**0**

Date: Sunday, September 27, 2015 Sheet 53 of 72

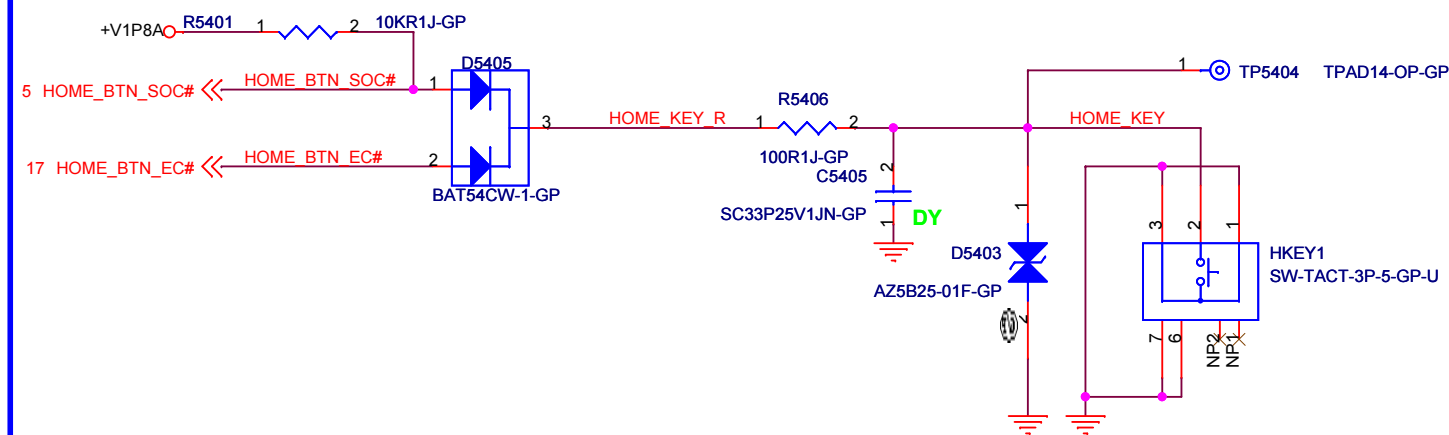
**PWR Button / Volum Key / Home key**



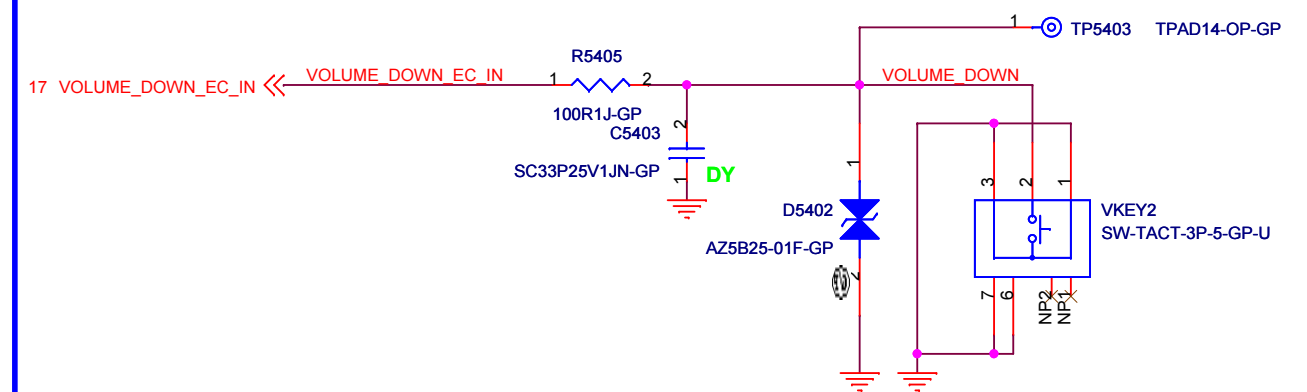
**VOLUME UP KEY**



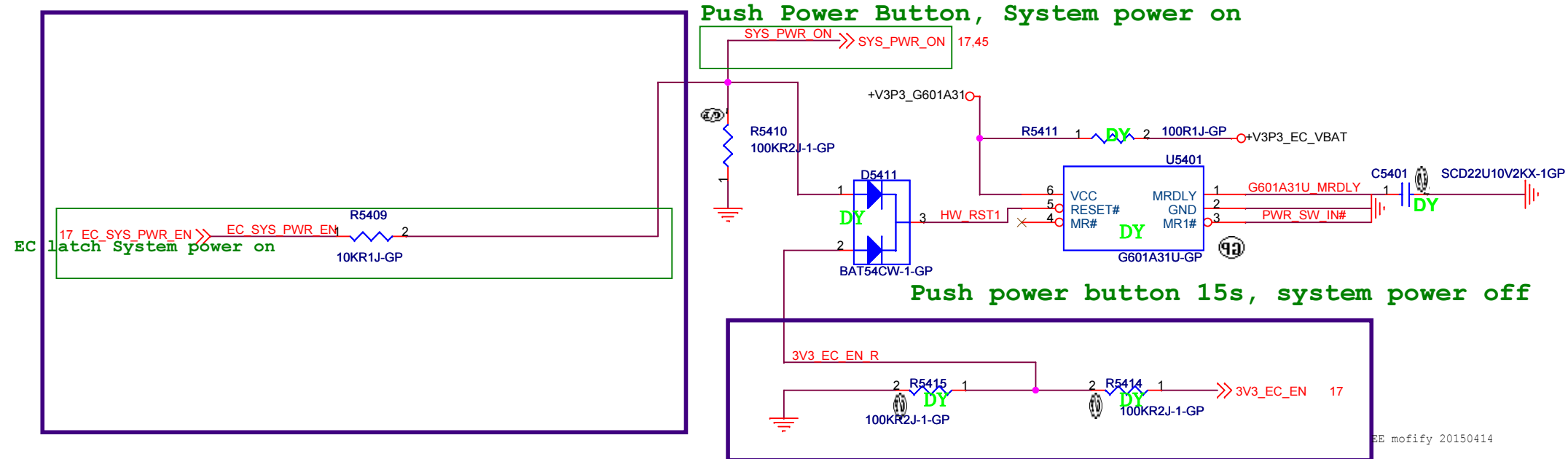
**HOME KEY**



VOLUME DOWN KEY



SYSTEM POWER ON



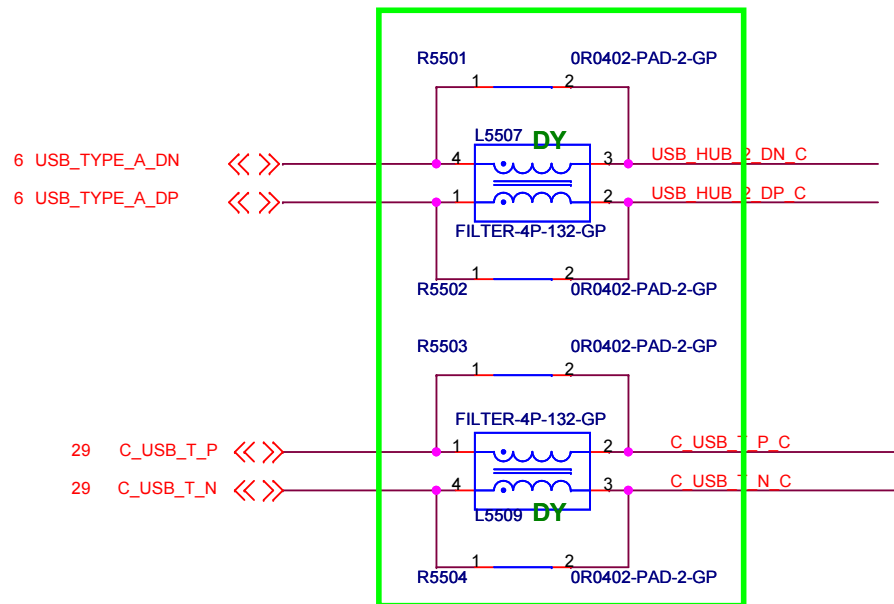
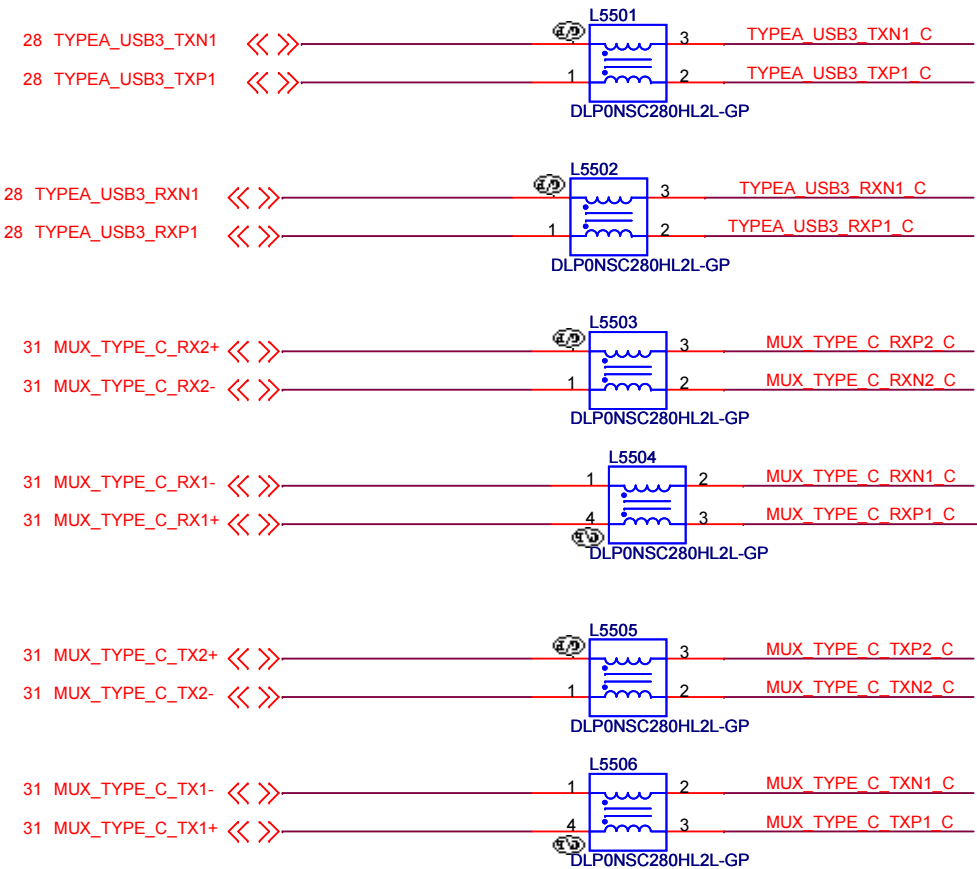
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Taipei Hsien 221, Taiwan, R.O.C.

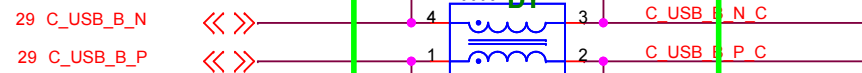
Title	<b>54_PWR/Volume/Home Button</b>
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Size	Document Number <b>Somerset</b>	Rev <b>SA</b>
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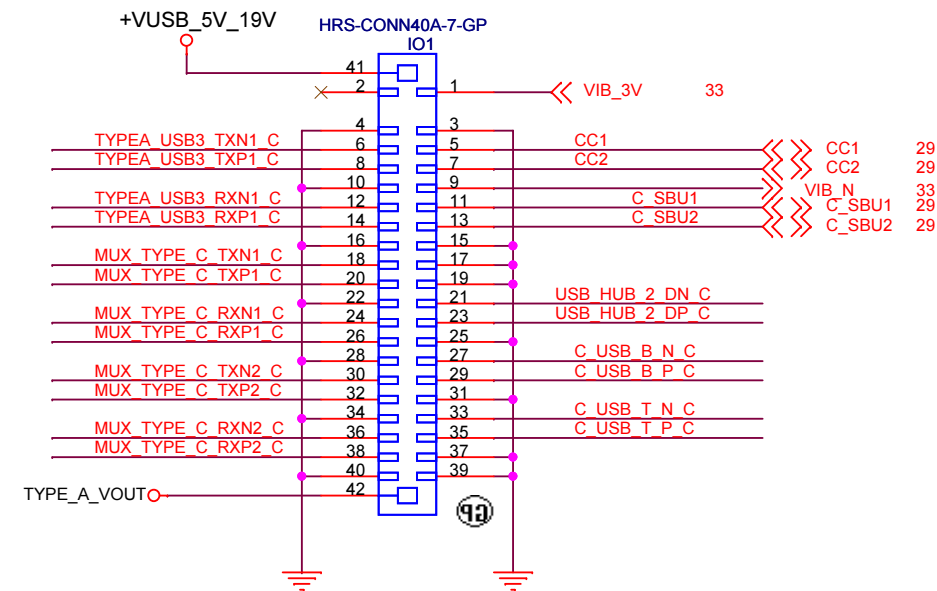
Date: Sunday, September 27, 2015 Sheet 54 of 72



EE modify 20150805



EE modify 20150805



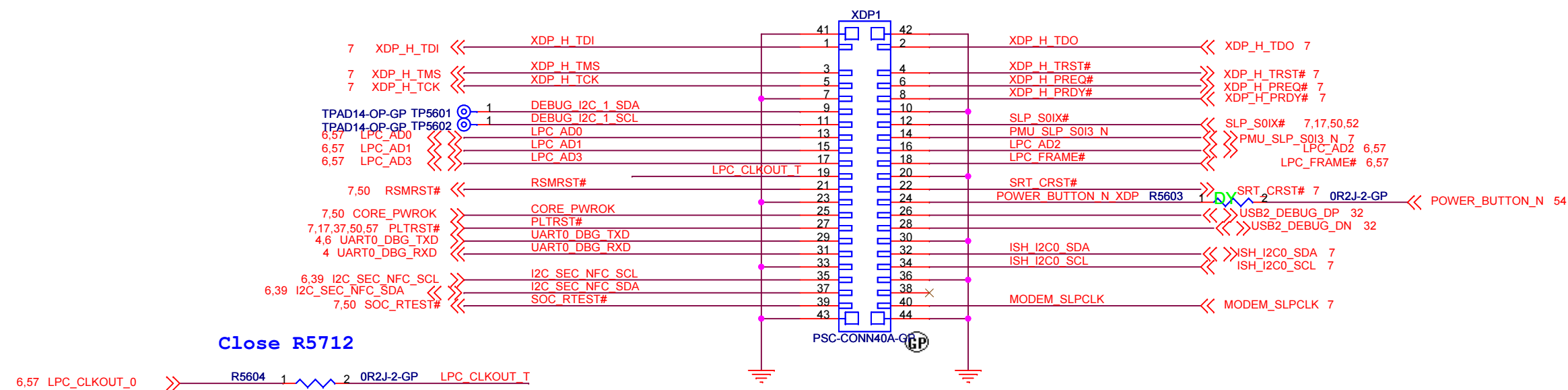
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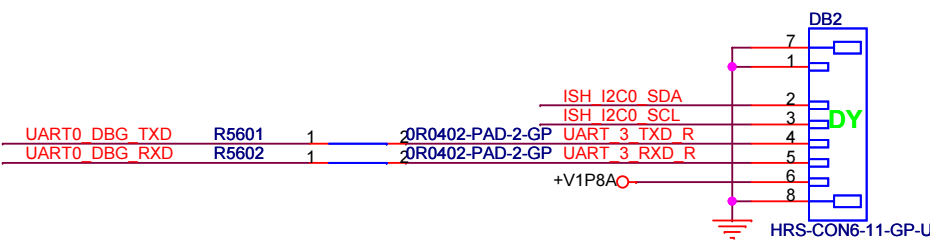
Title		
55_IO Board Connector		
Size	Document Number	Rev
	Somerset	SA
Date:	Sunday, September 27, 2015	Sheet 55 of 72

XDP Debug Connector

Debug Connector with XDP

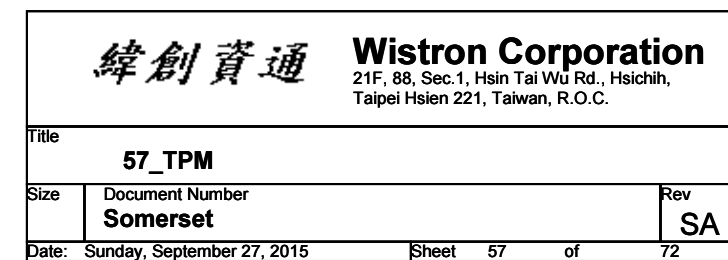


SW Debug Connector



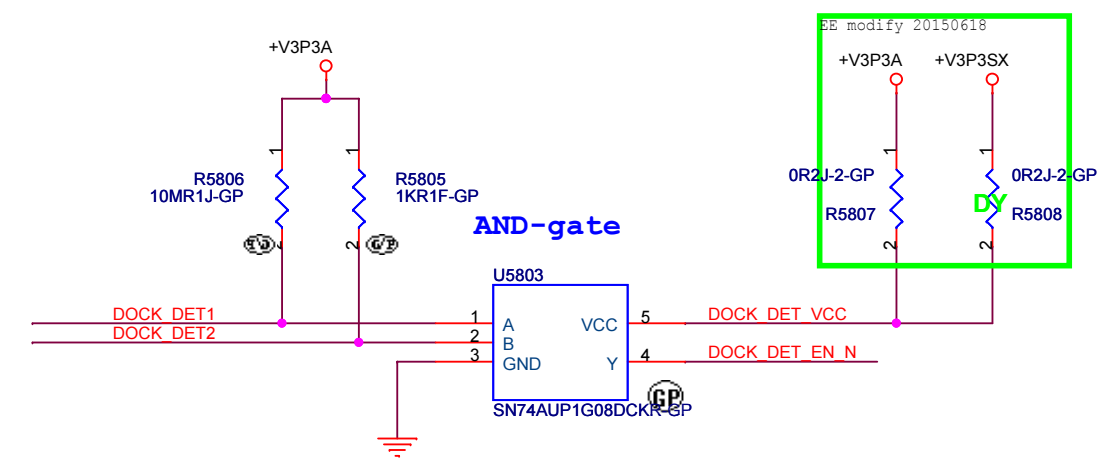
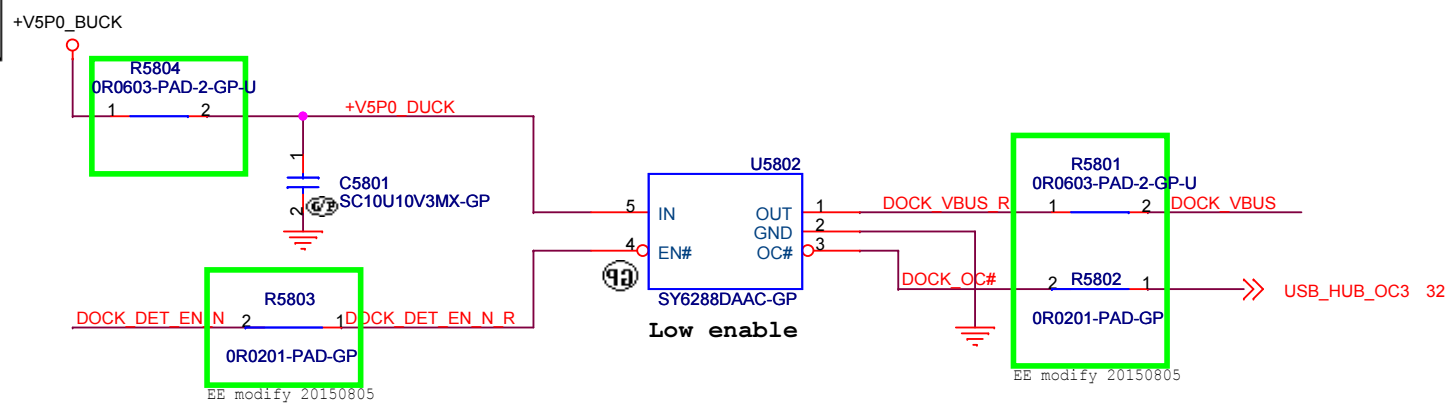
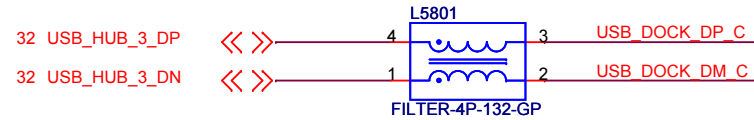
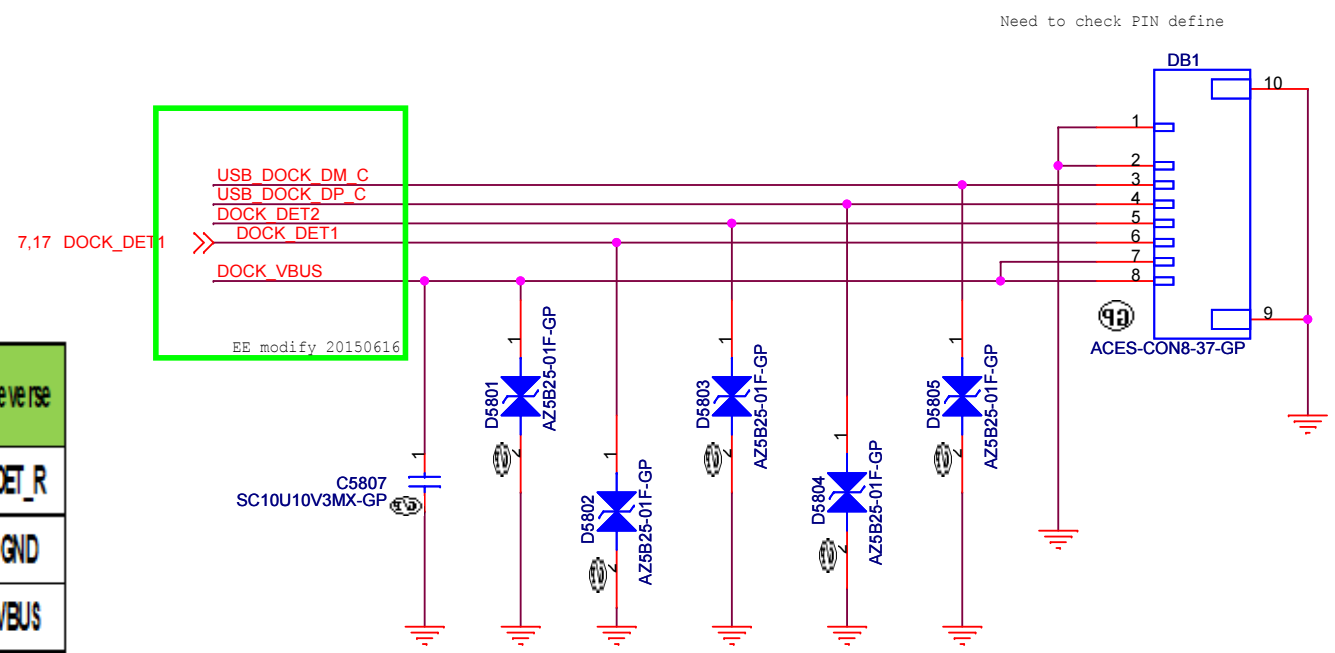
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Somerset



Docking CONN

PIN Number	POGO Pin Define	Reverse
1	DET_L	DET_R
2	GND	GND
3	VBUS	VBUS
4	USB1D-	USB2D+
5	USB1D+	USB1D-
6	VBUS	VBUS
7	GND	GND
8	DET_R	DET_L



	Before		After	
Detect Pin	DET1	DET2	DET1	DET2
Un Dock	H	H	H	H
Dock	H	L	L	H
Reverse Dock	L	L	H	L


	Before		After	
MB	R5805	R5806	R5805	R5806
Value	51Kohm	51Kohm	1Kohm	10Mohm
Dock	R2	R7	R2	R7
Value	0	1.8Mohm	0	1.4Kohm

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5	4	3	2	1
D				D
C				C
B				B
A				A

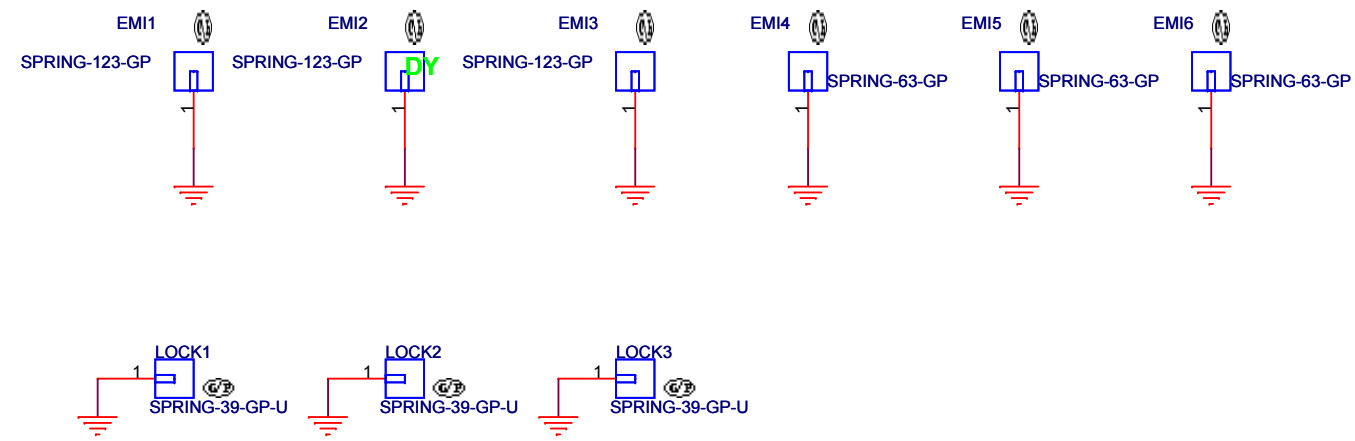
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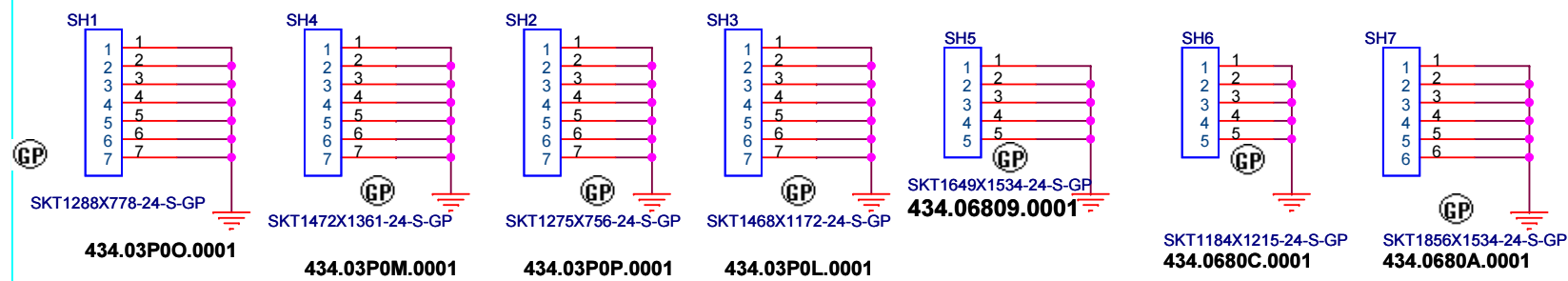
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>59_CPU_XDP</b>		
Size	Document Number <b>Somerset</b>	Rev <b>SA</b>
Date:	Sunday, September 27, 2015	Sheet 59 of 72



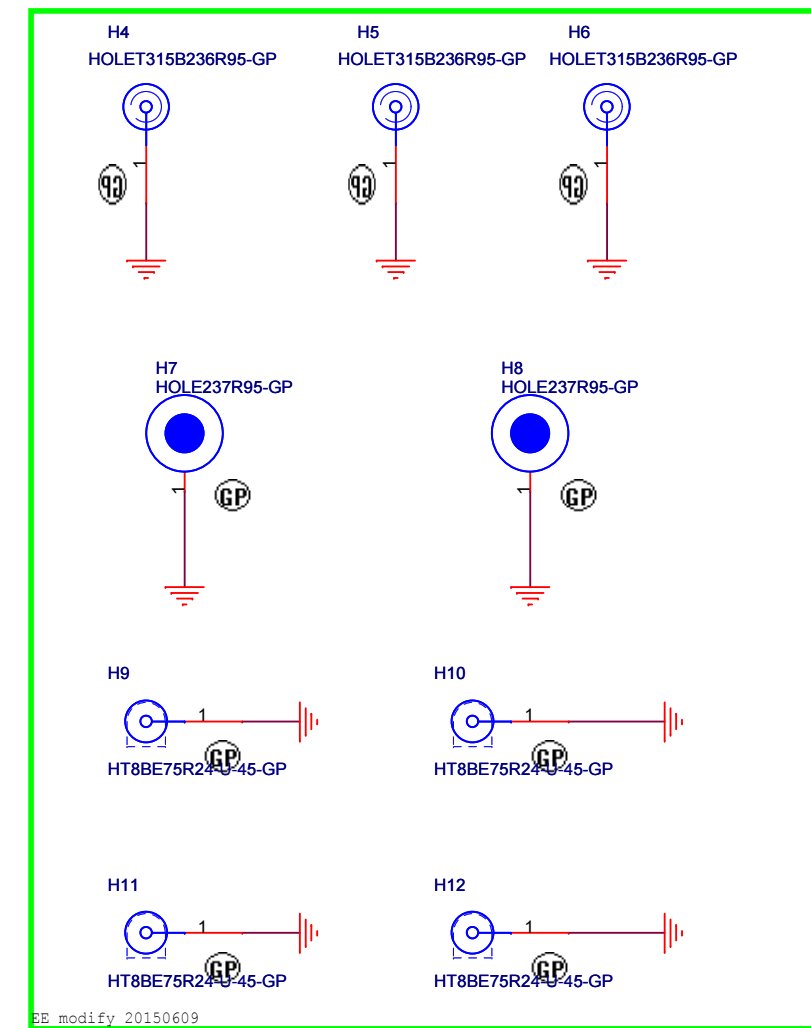
## Spring



## Shielding Can



## Screw Hole



EE modify 20150609

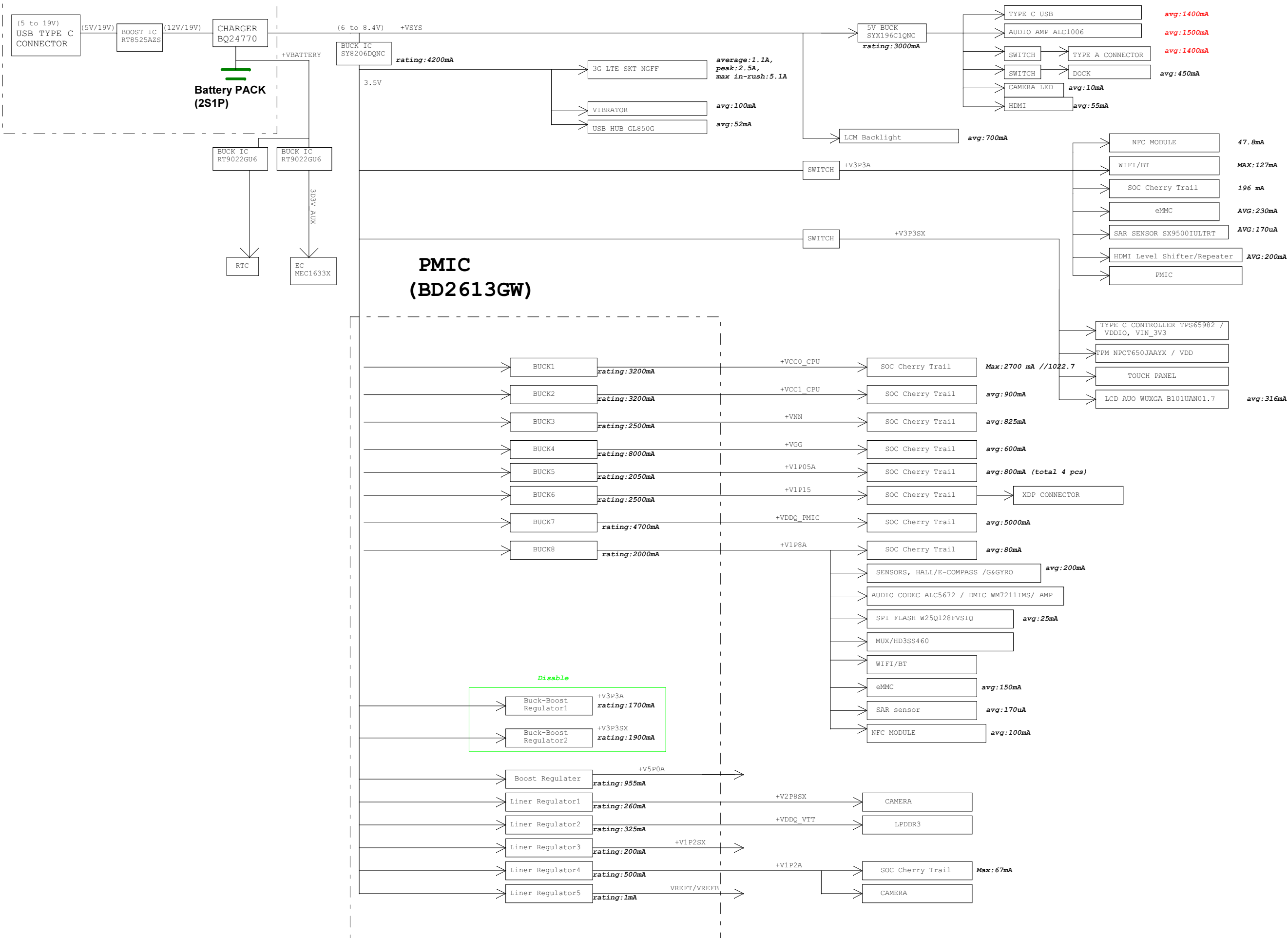
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Title			
60_ME/EMI			
Size	Document Number		Rev
	Somerset		SA
Date:	Sunday, September 27, 2015		Sheet 60 of 72

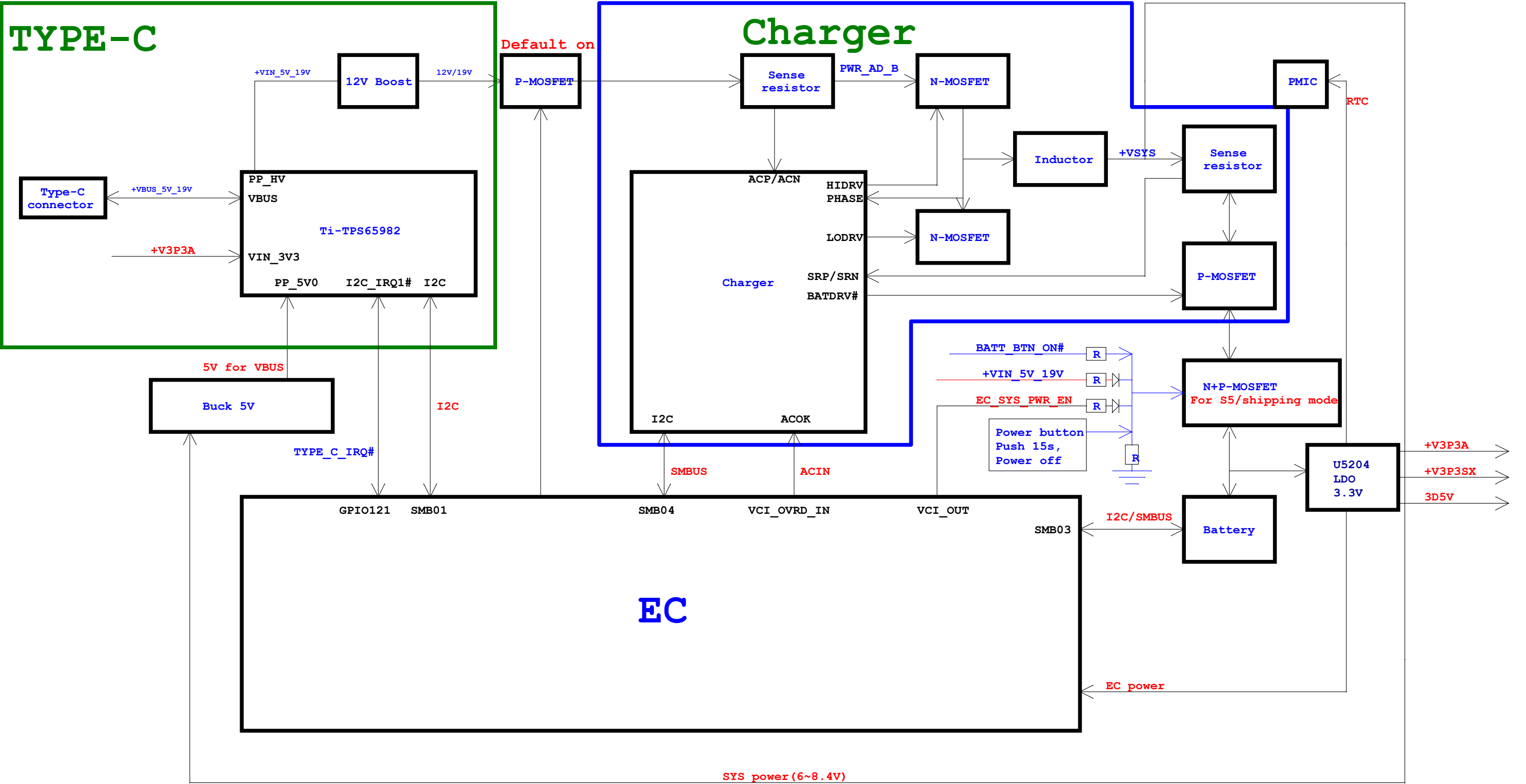
5					4					3					2					1				
D																								
C																								
B																								

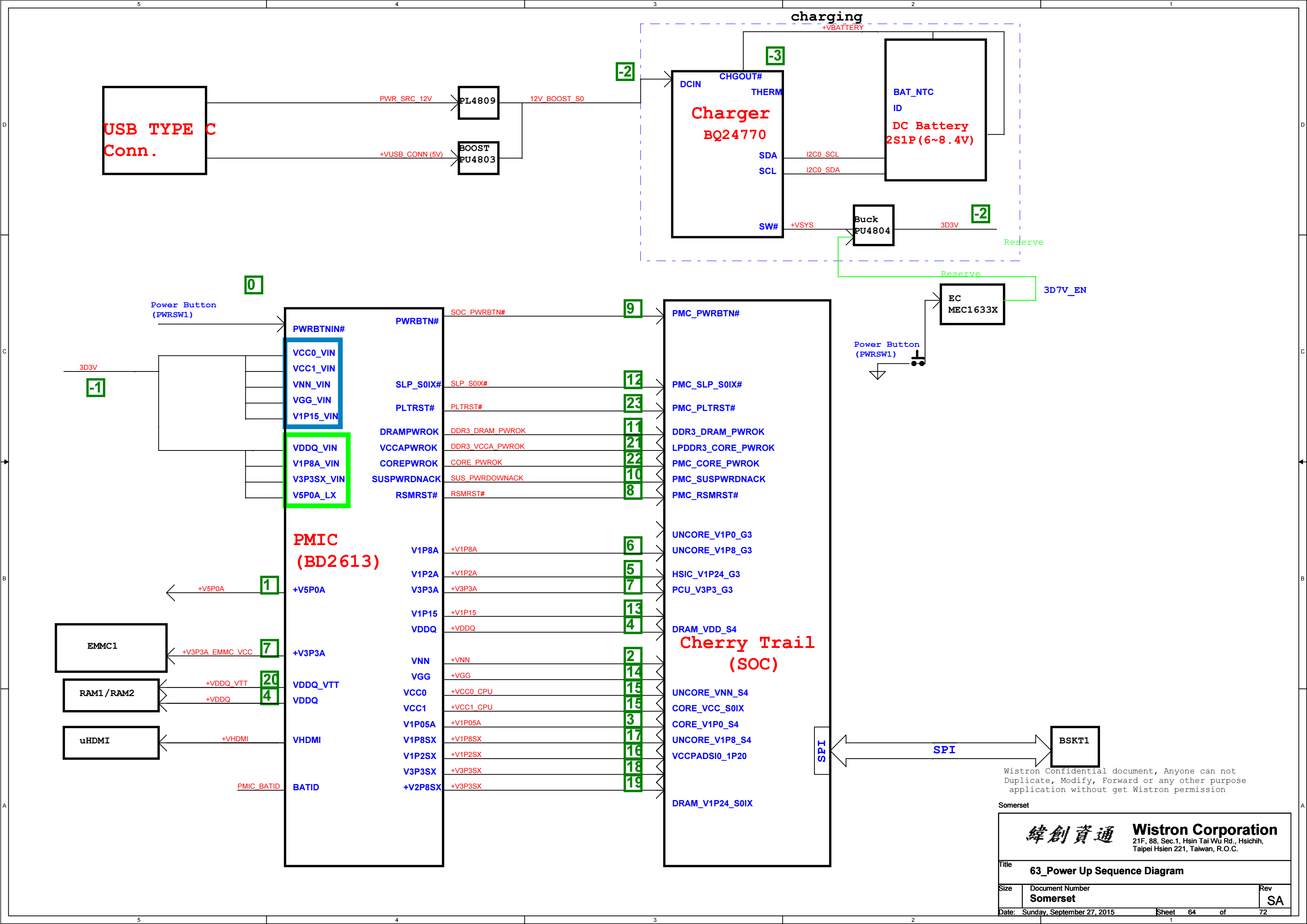
# SOC Cherry Trail POWERMAP



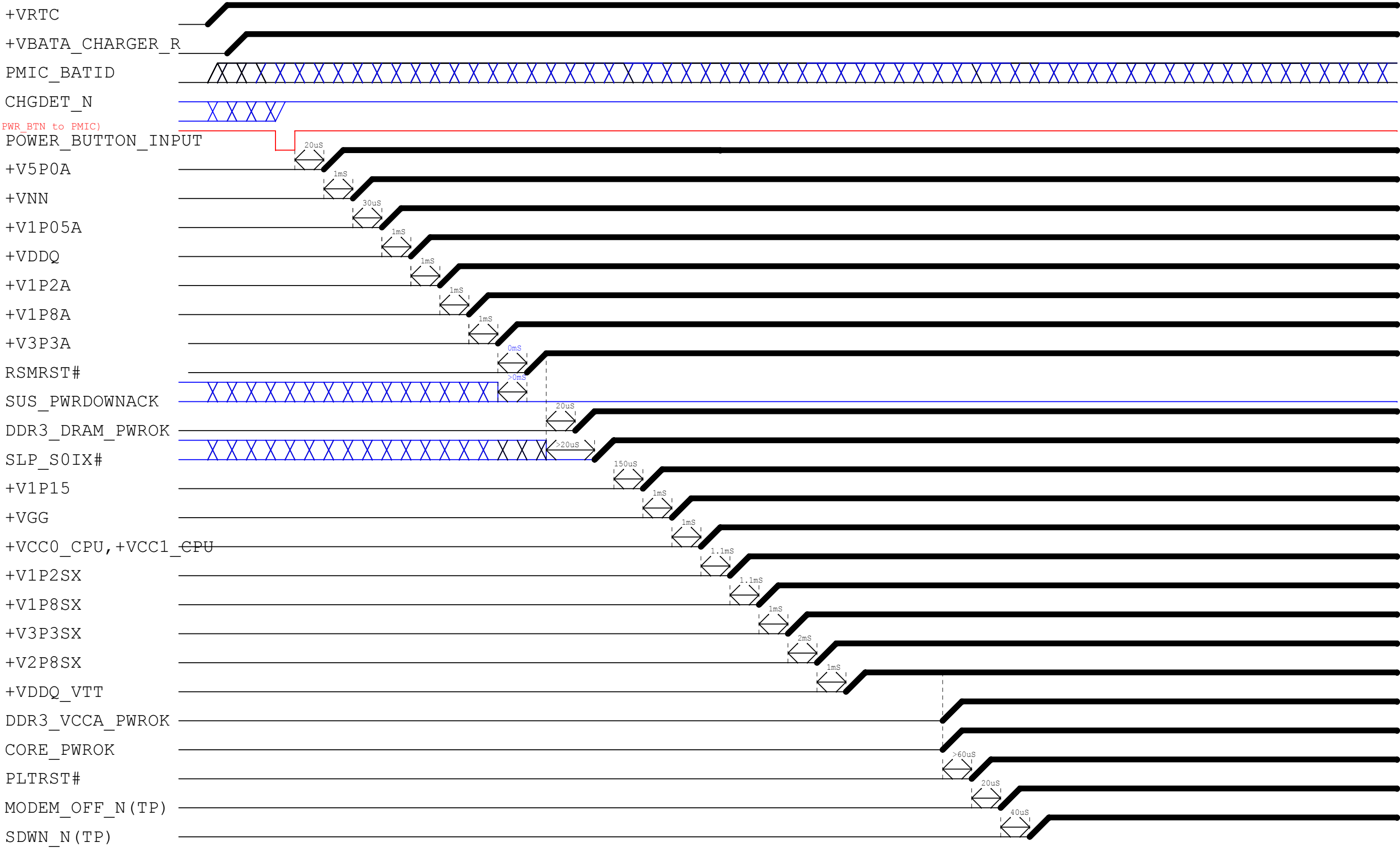
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# Power block diagram



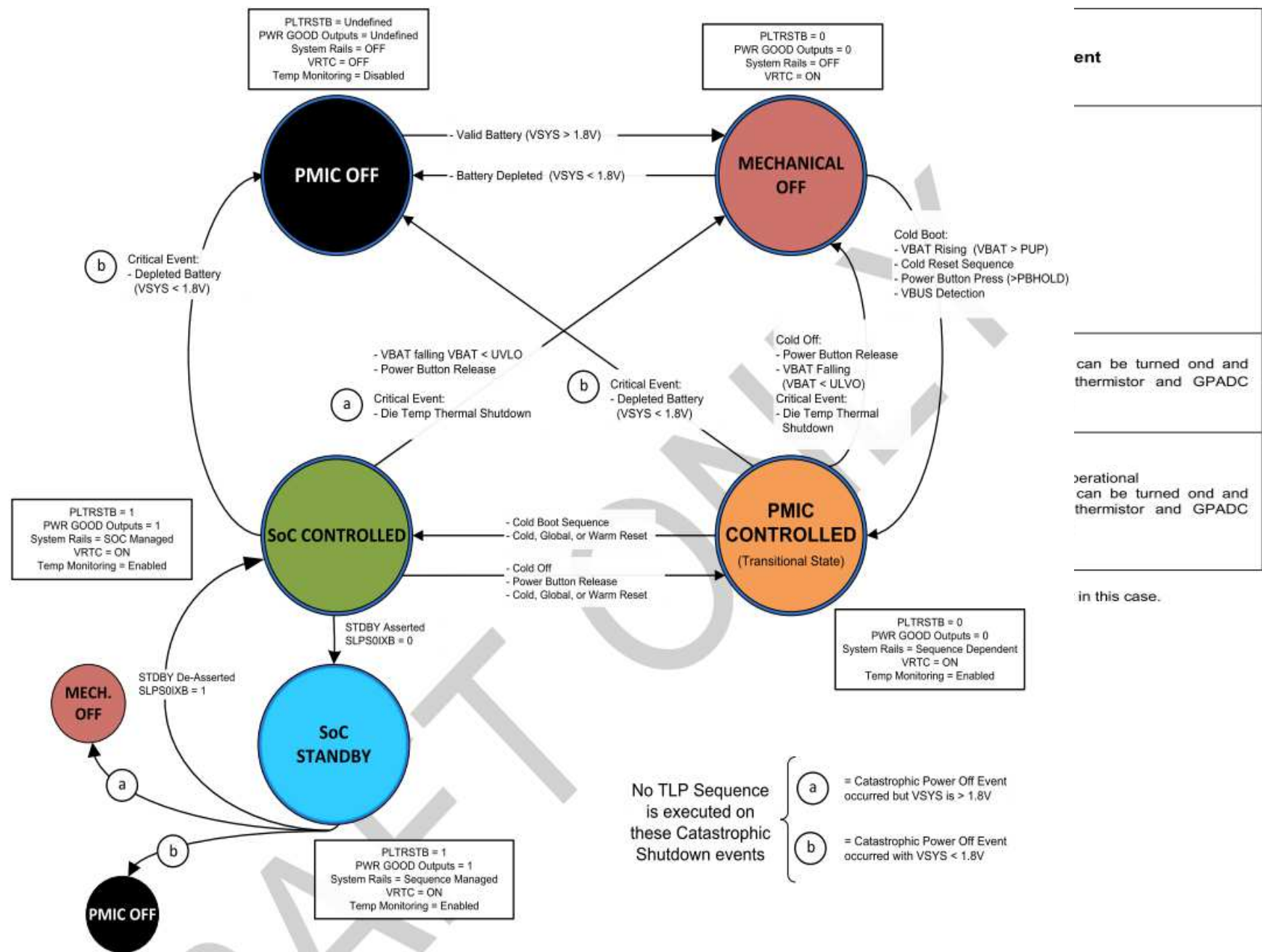


CherryTrail Platform Power Sequencing:Cold Boot (Power Up)



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Somerset



	PART	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5	BUCK6	LD01	LD02	LD03	VRTC	LD04	VREFDQ	LD05	LD06	LD07	LD08	LD09	LD010	LD011	LD012	LD013	LD014	Comment
PMIC OFF	BYT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
	CHT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Mechanical Off	BYT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
	CHT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
SoC Controlled	BYT	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Disabled by default. SoC can enable/disable according to system activity
	CHT	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Disabled by default. SoC can enable/disable according to system activity
SoC Standby	BYT	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Will keep whatever state had before entering standby
	CHT	OFF	ON	V_SLEEP	V_SLEEP	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Will keep whatever state had before entering standby

LDO7-LDO14 will keep whatever state before entering standby, it's up to the user whether to enable/disable. State machine won't enforce the behavior in this case.

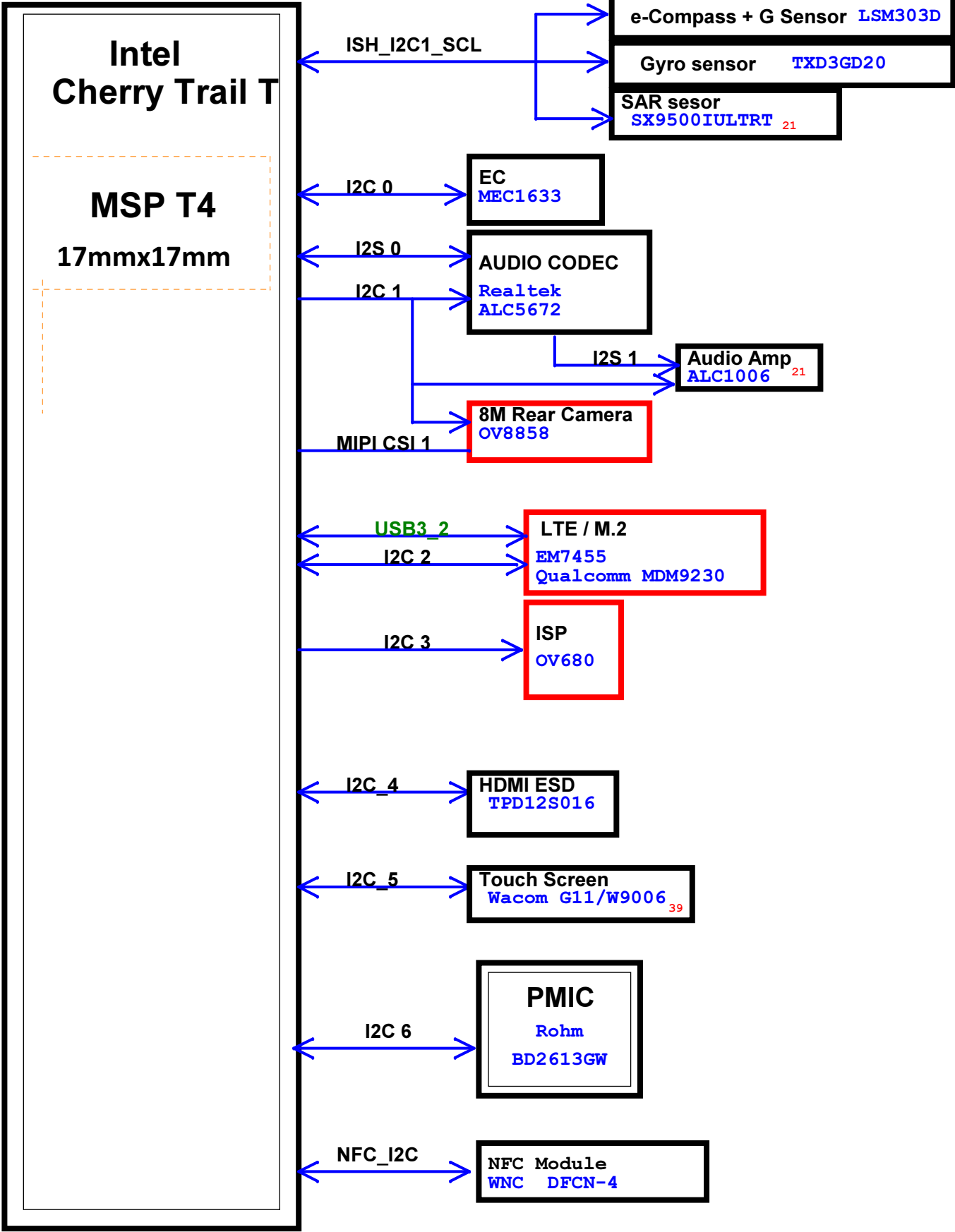
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Title <b>65_Power State</b>			
Size	Document Number		Rev
	<b>Somerset</b>		<b>SA</b>
Date:	Sunday, September 27, 2015		Sheet 66 of 72



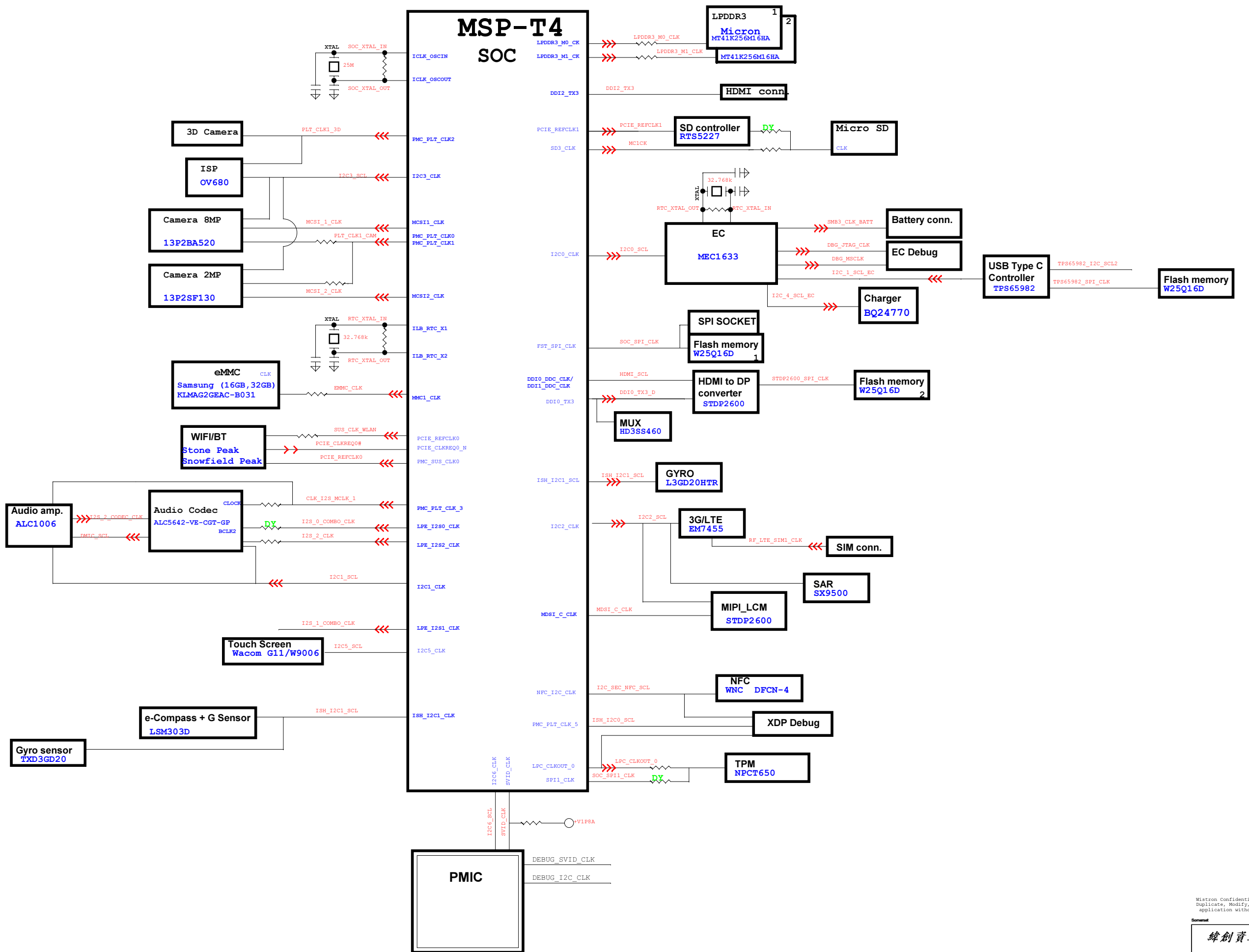
I2C Block Diagram

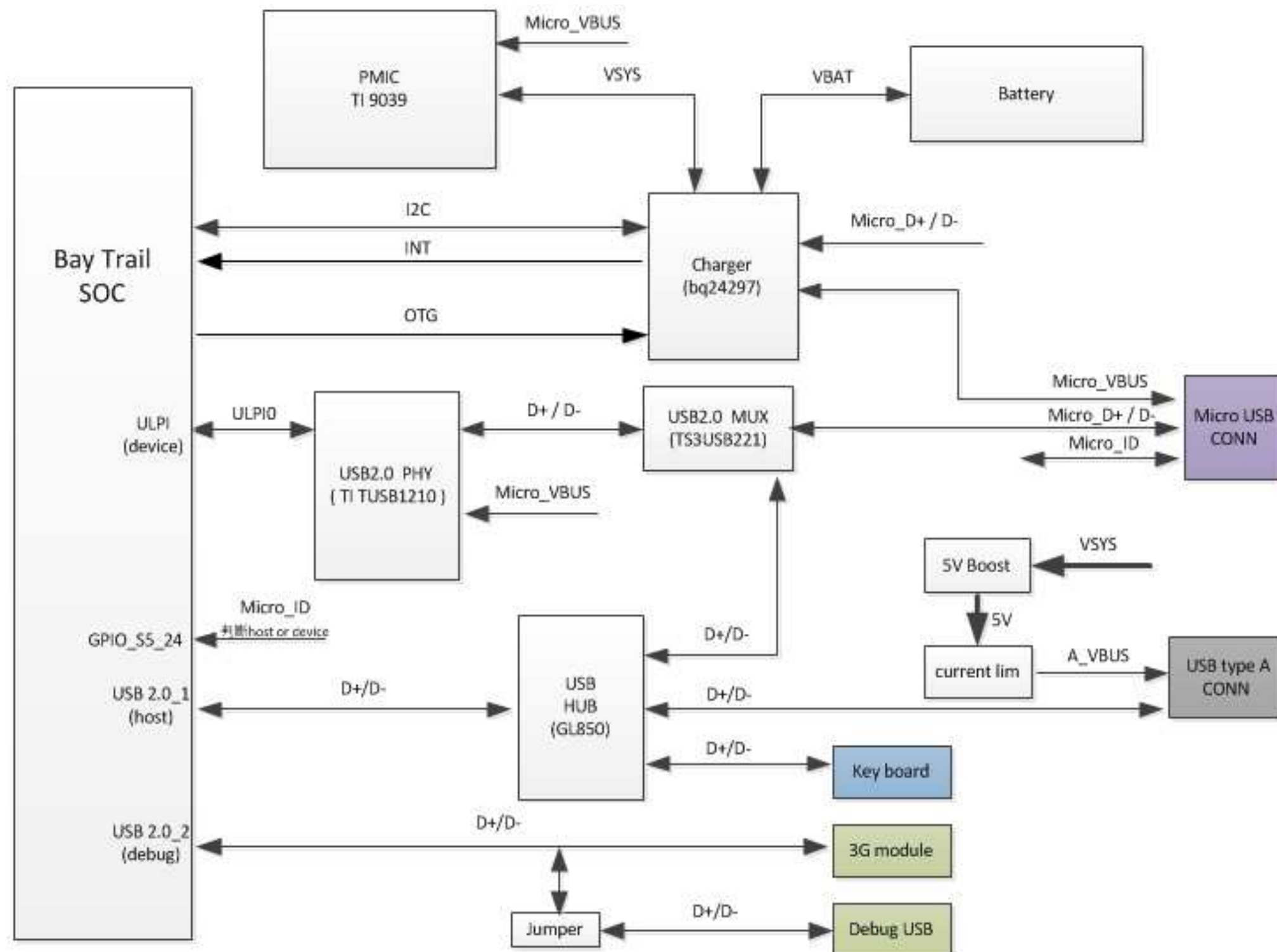


I2C	Function	Device	address(7-bits)
ISH_I2C1_SCL	e-Compass + G Sensor	LSM303D	0x1E
	Gyro sensor	L3GD20HTR	0x6B
	SAR sesor	SX9500	0x28
0	EC	MEC1633X	
1	AUDIO CODEC	ALC5672	1CH
2	8M Rear Camera	OV8858	
3	LTE / M.2	EM7455	
4	ISP	OV680	0x35
5	HDMI ESD	TPD12S016	
6	Touch Screen	Wacom G11/W9006	
6	PMIC	BD2613GW	06E
NFC_I2C	NFC	WNC DFCN-4	29H

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CLOCK Block Diagram

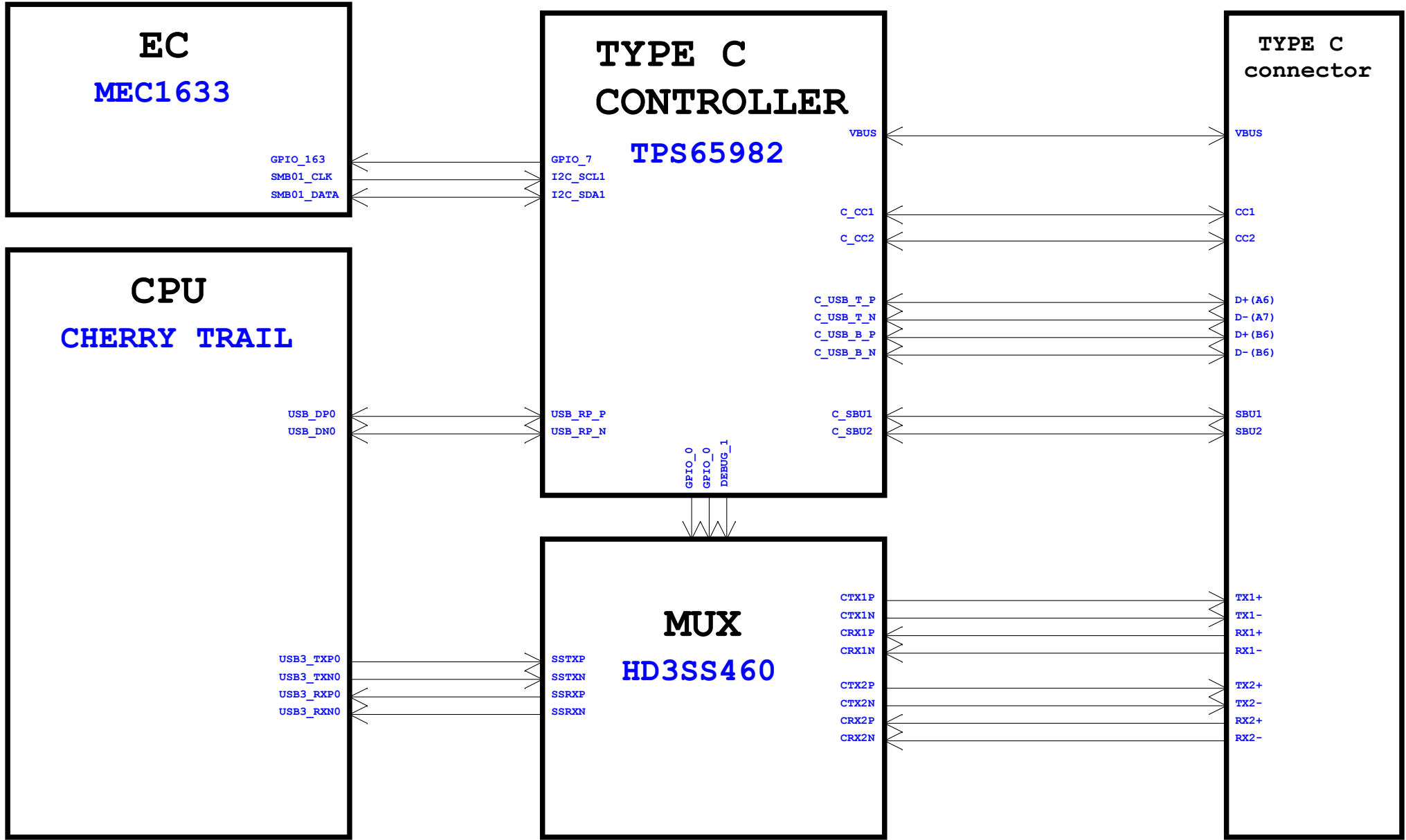




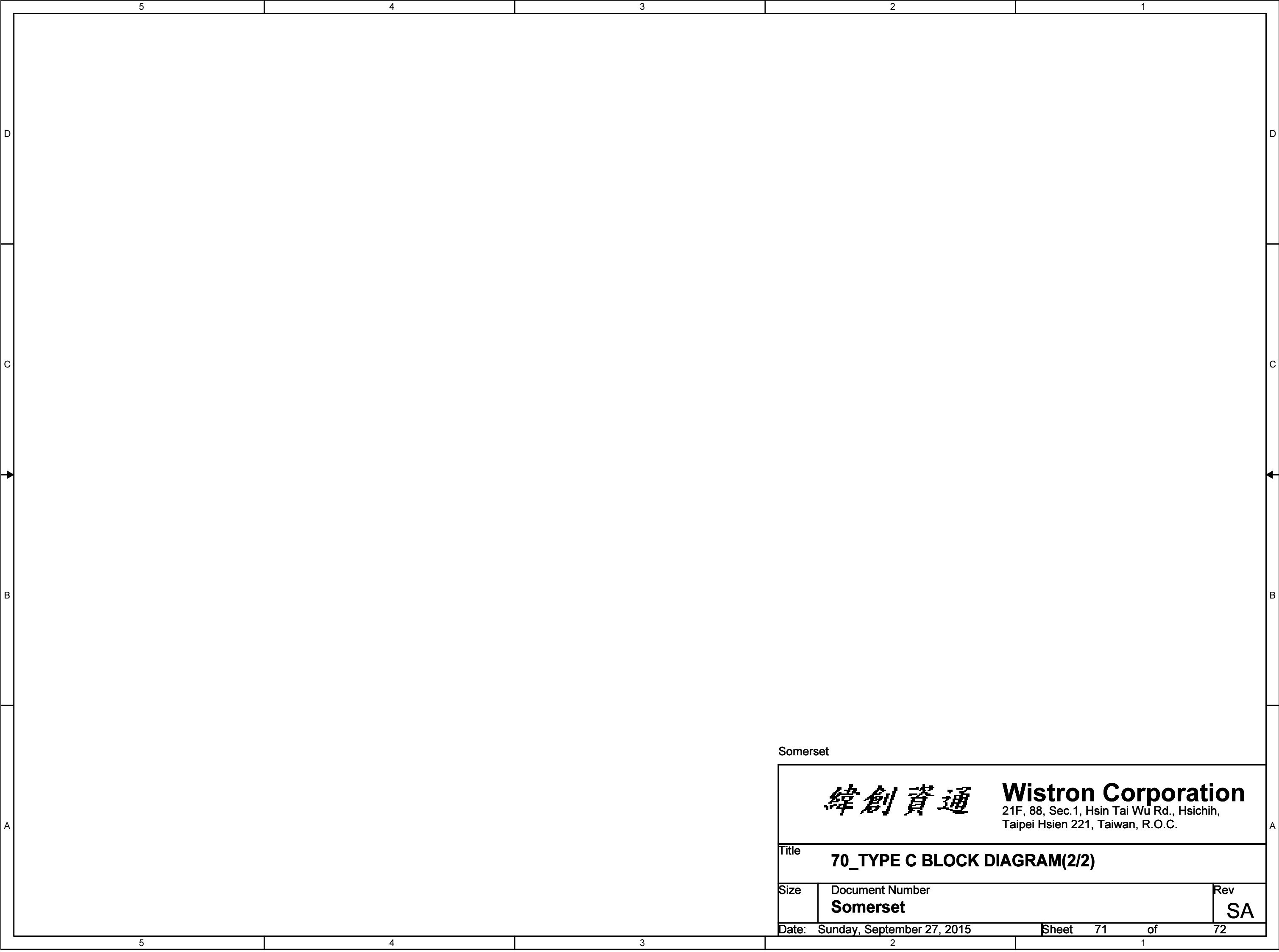
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<div> <div>緯創資通</div> <div> <b>Wistron Corporation</b>            21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,            Taipei Hsien 221, Taiwan, R.O.C.         </div> </div>	
Title <b>68_USB IO BLOCK DIAGRAM</b>	
Size	Document Number <b>Somerset</b>
Date: Sunday, September 27, 2015	Rev <b>SA</b>
Sheet 69 of 72	




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Reversion History

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Title <b>71_Change History</b>			
Size	Document Number <b>Somerset</b>		Rev <b>SA</b>
Date: Sunday, September 27, 2015		Sheet 72	of 72